SN74AUP1G79 Low-Power Single Positive-Edge-Triggered D-Type Flip-Flop

1 Features

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption: I_{CC} = 0.9 µA Maximum
- Low Dynamic-Power Consumption: C_{pd} = 3 pF Typical at 3.3 V
- Low Input Capacitance: C_i = 1.5 pF Typical
- Low Noise: Overshoot and Undershoot < 10% of V_{CC}
- I_{off} Supports Partial Power-Down-Mode Operation
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typical at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- t_{pd} = 4 ns Maximum at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Barcode Scanner
- Cable Solutions
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning
- Network-Attached Storage (NAS)
- Server Motherboard and PSU
- Software Defined Radio (SDR)
- TV: High-Definition (HDTV), LCD, and Digital
- Video Communications System
- Wireless Data Access Card, Headset, Keyboard, Mouse, and LAN Card

3 Description

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family assures a very-low static and dynamic power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, thus resulting in an increased battery life. The AUP devices also maintain excellent signal integrity.

The SN74AUP1G79 is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup-time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

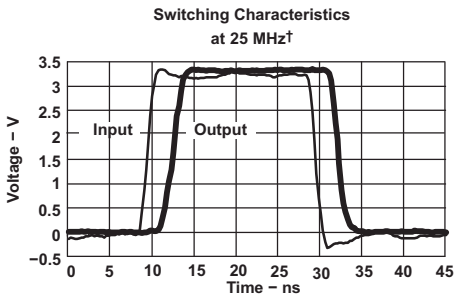
The SN74AUP1G79 device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AUP1G79DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74AUP1G79DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74AUP1G79DRL	SOT-5X3 (5)	1.60 mm × 1.20 mm
SN74AUP1G79DRY	SON (6)	1.45 mm × 1.00 mm
SN74AUP1G79DSF	SON (6)	1.00 mm × 1.00 mm
SN74AUP1G79DPW	X2SON (5)	0.80 mm x 0.80 mm
SN74AUP1G79YFP	DSBGA (6)	1.16 mm × 0.76 mm
SN74AUP1G79YZP	DSBGA (5)	1.39 mm × 0.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Power Consumption and Performance



† AUP1G08 data at C_L = 15 pF

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2015) to Revision I — **Page**

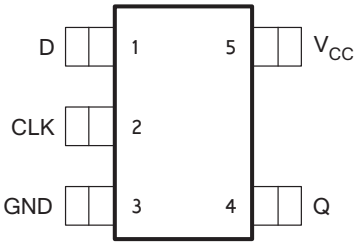
- Added DPW (X2SON) package ... 1
- Added Maximum junction temperature, T_J in *Absolute Maximum Ratings* ... 4
- Changed values in the *Thermal Information* table to align with JEDEC standards. ... 5
- Added *Balanced High-Drive CMOS Push-Pull Outputs*, *Standard CMOS Inputs*, *Clamp Diodes*, *Partial Power Down (I_{off})*, *Over-voltage Tolerant Inputs* ... 15
- Added *Receiving Notification of Documentation Updates* and *Community Resources* ... 20

Changes from Revision G (May 2010) to Revision H — **Page**

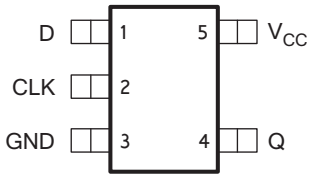
- Updated document to the new TI data sheet format ... 1
- Removed *Ordering Information* table ... 1
- Added *Device Information* table ... 1
- Added *Typical Characteristics* section ... 12

5 Pin Configuration and Functions

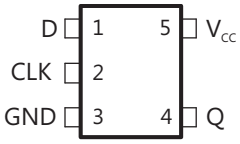
DBV Package
5-Pin SOT-23
Top View



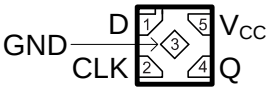
DCK Package
5-Pin SC70
Top View



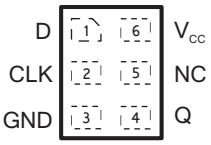
DRL Package
5-Pin SOT-5X3
Top View



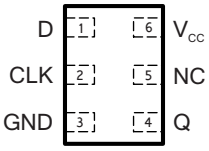
DPW Package
5-Pin X2SON
Top View



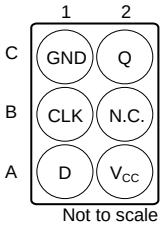
DRY Package
6-Pin SON
Top View



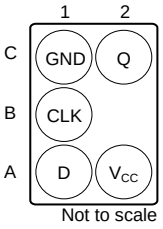
DSF Package
6-Pin SON
Top View



YFP Package
6-Pin DSBGA
Bottom View



YZP Package
5-Pin DSBGA
Bottom View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YFP		
CLK	2	2	B1	B1	I	Positive-Edge-Triggered Clock input
D	1	1	A1	A1	I	Data Input
GND	3	3	C1	C1	—	Ground pin
NC	—	5	—	B2	—	No Connect
Q	4	4	C2	C2	O	Q output
V_{CC}	5	6	A2	A2	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Output voltage range in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Maximum junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage (1)		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 0.8 V		–20	µA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65 V		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to assure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.4 Thermal Information

THERMAL METRIC (1)		SN74AUP1G79								UNIT
		DBV (SOT-23)	DCK (SC70)	DRL (SOT-5X3)	DRY (SON)	DSF (SON)	DPW (X2SON)	YFP (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	267.2	284.1	294.1	341.1	377.1	489.2	125.4	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	191.9	208.5	132.5	233.1	187.7	226.3	1.9	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.1	103.1	143.4	206.7	236.6	352.9	37.2	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	83.0	76.6	14.5	63.4	29.0	38.2	0.5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	100.8	102.3	143.9	206.7	236.3	352.1	37.5	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	150.8	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: T_A = 25°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –20 µA	0.8 V to 3.6 V	V_{CC} – 0.1			V
	I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			
	I_{OH} = –1.7 mA	1.4 V	1.11			
	I_{OH} = –1.9 mA	1.65 V	1.32			
	I_{OH} = –2.3 mA	2.3 V	2.05			
	I_{OH} = –3.1 mA		1.9			
	I_{OH} = –2.7 mA	3 V	2.72			
	I_{OH} = –4 mA		2.6			
V_{OL}	I_{OL} = 20 µA	0.8 V to 3.6 V			0.1	V
	I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}	
	I_{OL} = 1.7 mA	1.4 V			0.31	
	I_{OL} = 1.9 mA	1.65 V			0.31	
	I_{OL} = 2.3 mA	2.3 V			0.31	
	I_{OL} = 3.1 mA				0.44	
	I_{OL} = 2.7 mA	3 V			0.31	
	I_{OL} = 4 mA				0.44	
I_I D or CLK input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1	µA
I_{off}	V_I or V_O = 0 V to 3.6 V	0 V			0.2	µA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2	µA
I_{CC}	V_I = GND or V_{CC} to 3.6 V, I_O = 0	0.8 V to 3.6 V			0.5	µA
ΔI_{CC}	V_I = V_{CC} – 0.6 V,(1) I_O = 0	3.3 V			40	µA
C_i	V_I = V_{CC} or GND	0 V		1.5		pF
		3.6 V		1.5		
C_o	V_O = GND	0 V		3		pF

(1) One-input switching

6.6 Electrical Characteristics: T_A = –40°C to 85°C

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	MAX	UNIT
V_{OH}	I_{OH} = –20 µA		0.8 V to 3.6 V	V_{CC} – 0.1		V
	I_{OH} = –1.1 mA		1.1 V	0.7 × V_{CC}		
	I_{OH} = –1.7 mA		1.4 V	1.03		
	I_{OH} = –1.9 mA		1.65 V	1.3		
	I_{OH} = –2.3 mA		2.3 V	1.97		
	I_{OH} = –3.1 mA			1.85		
	I_{OH} = –2.7 mA		3 V	2.67		
	I_{OH} = –4 mA			2.55		
V_{OL}	I_{OL} = 20 µA		0.8 V to 3.6 V		0.1	V
	I_{OL} = 1.1 mA		1.1 V		0.3 × V_{CC}	
	I_{OL} = 1.7 mA		1.4 V		0.37	
	I_{OL} = 1.9 mA		1.65 V		0.35	
	I_{OL} = 2.3 mA		2.3 V		0.33	
	I_{OL} = 3.1 mA				0.45	
	I_{OL} = 2.7 mA		3 V		0.33	
	I_{OL} = 4 mA				0.45	
I_I D or CLK input	V_I = GND to 3.6 V		0 V to 3.6 V		0.5	µA
I_{off}	V_I or V_O = 0 V to 3.6 V		0 V		0.6	µA
ΔI_{off}	V_I or V_O = 0 V to 3.6 V		0 V to 0.2 V		0.6	µA
I_{CC}	V_I = GND or V_{CC} to 3.6 V,	I_O = 0	0.8 V to 3.6 V		0.9	µA
ΔI_{CC}	V_I = V_{CC} – 0.6 V,(1)	I_O = 0	3.3 V		50	µA

(1) One-input switching

6.7 Timing Requirements

over recommended operating free-air temperature range, T_A = –40°C to +85°C (unless otherwise noted) (see Figure 3)

			V_{CC}	MIN	TYP(1)	MAX	UNIT
f_{clock}	Clock frequency		0.8 V			20	MHz
			1.2 V ± 0.1 V			80	
			1.5 V ± 0.1 V			100	
			1.8 V ± 0.15 V			140	
			2.5 V ± 0.2 V			210	
			3.3 V ± 0.3 V			260	
t_w	Pulse duration, CLK high or low		0.8 V	4.8			ns
			1.2 V ± 0.1 V	2.2			
			1.5 V ± 0.1 V	1.5			
			1.8 V ± 0.15 V	1.6			
			2.5 V ± 0.2 V	1.7			
			3.3 V ± 0.3 V	1.9			
t_{su}	Setup time before CLK↑	Data high	0.8 V	4.2	2.9		ns
			1.2 V ± 0.1 V	1.4			
			1.5 V ± 0.1 V	1			
			1.8 V ± 0.15 V	0.9			
			2.5 V ± 0.2 V	0.7			
			3.3 V ± 0.3 V	0.6			
		Data low	0.8 V	5.3	3.5		
			1.2 V ± 0.1 V	1.8			
			1.5 V ± 0.1 V	1.2			
			1.8 V ± 0.15 V	1.1			
			2.5 V ± 0.2 V	1			
			3.3 V ± 0.3 V	1			
t_h	Hold time, data after CLK↑		0.8 V	0	0		ns
			1.2 V ± 0.1 V	0			
			1.5 V ± 0.1 V	0			
			1.8 V ± 0.15 V	0			
			2.5 V ± 0.2 V	0			
			3.3 V ± 0.3 V	0			

(1) T_A = 25°C

6.8 Switching Characteristics: C_L = 5 pF

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			V_{CC} = 0.8 V	T_A = 25°C		93		MHz
				T_A = –40°C to +85°C	90			
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C		199		
				T_A = –40°C to +85°C	220			
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C		250		
				T_A = –40°C to +85°C	230			
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C		271		
				T_A = –40°C to +85°C	240			
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C		280		
				T_A = –40°C to +85°C	250			
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C		280		
				T_A = –40°C to +85°C	260			
t_{pd}	CLK	Q	V_{CC} = 0.8 V	T_A = 25°C		15.9		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	3.7	6.9	11	
				T_A = –40°C to +85°C	2.6		13.1	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	3	4.8	7.6	
				T_A = –40°C to +85°C	2		8.8	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	2.4	3.8	6.1	
				T_A = –40°C to +85°C	1.5		7.1	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	1.8	2.7	4.4	
				T_A = –40°C to +85°C	1.1		5	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1.5	2.1	3.6	
				T_A = –40°C to +85°C	0.9		4	

6.9 Switching Characteristics: C_L = 10 pF

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			V_{CC} = 0.8 V	T_A = 25°C		62		MHz
				T_A = –40°C to +85°C	50			
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C		147		
				T_A = –40°C to +85°C	160			
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C		189		
				T_A = –40°C to +85°C	200			
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C		180		
				T_A = –40°C to +85°C	240			
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C		260		
				T_A = –40°C to +85°C	250			
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C		280		
				T_A = –40°C to +85°C	260			

Switching Characteristics: C_L = 10 pF (continued)

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd}	CLK	Q	V_{CC} = 0.8 V	T_A = 25°C		18		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	4.3	7.8	12.3	
				T_A = –40°C to +85°C	3.2		14.4	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	3.5	5.5	8.4	
				T_A = –40°C to +85°C	2.5		9.8	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	2.8	4.4	6.8	
				T_A = –40°C to +85°C	1.9		8	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	2.2	3.2	5	
				T_A = –40°C to +85°C	1.5		5.7	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	1.8	2.6	4.1	
				T_A = –40°C to +85°C	1.3		4.5	

6.10 Switching Characteristics: C_L = 15 pF

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			V_{CC} = 0.8 V	T_A = 25°C		48		MHz
				T_A = –40°C to +85°C	30			
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C		112		
				T_A = –40°C to +85°C	120			
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C		151		
				T_A = –40°C to +85°C	160			
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C		194		
				T_A = –40°C to +85°C	220			
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C		248		
				T_A = –40°C to +85°C	250			
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C		280		
				T_A = –40°C to +85°C	260			
t_{pd}	CLK	Q	V_{CC} = 0.8 V	T_A = 25°C		20.3		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	5	8.7	13.6	
				T_A = –40°C to +85°C	3.9		15.6	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	4.1	6.3	9.3	
				T_A = –40°C to +85°C	3.1		10.7	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	3.3	4	7.6	
				T_A = –40°C to +85°C	2.4		8.7	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	2.6	3.6	5.5	
				T_A = –40°C to +85°C	1.9		6.3	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	2.2	3	4.5	
				T_A = –40°C to +85°C	1.6		5	

6.11 Switching Characteristics: C_L = 30 pF

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			V_{CC} = 0.8 V	T_A = 25°C		24		MHz
				T_A = –40°C to +85°C	20			
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C		72		
				T_A = –40°C to +85°C	80			
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C		100		
				T_A = –40°C to +85°C	100			
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C		127		
				T_A = –40°C to +85°C	140			
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C		185		
				T_A = –40°C to +85°C	210			
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C		266		
				T_A = –40°C to +85°C	260			
t_{pd}	CLK	Q	V_{CC} = 0.8 V	T_A = 25°C		27.2		ns
			V_{CC} = 1.2 V ± 0.1 V	T_A = 25°C	7	11.5	17.3	
				T_A = –40°C to +85°C	5.9		24	
			V_{CC} = 1.5 V ± 0.1 V	T_A = 25°C	5.7	8.3	11.8	
				T_A = –40°C to +85°C	4.6		15.9	
			V_{CC} = 1.8 V ± 0.15 V	T_A = 25°C	4.7	6.7	9.6	
				T_A = –40°C to +85°C	3.8		13	
			V_{CC} = 2.5 V ± 0.2 V	T_A = 25°C	3.7	4.9	7	
				T_A = –40°C to +85°C	2.9		9	
			V_{CC} = 3.3 V ± 0.3 V	T_A = 25°C	3.2	4.1	5.8	
				T_A = –40°C to +85°C	2.6		7.2	

6.12 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	2.5	pF
			1.2 V ± 0.1 V	2.5	
			1.5 V ± 0.1 V	2.5	
			1.8 V ± 0.15 V	2.5	
			2.5 V ± 0.2 V	3	
			3.3 V ± 0.3 V	3	

6.13 Typical Characteristics

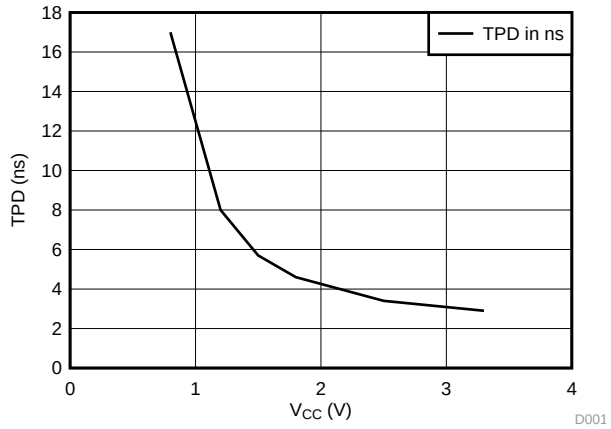


Figure 1. TPD vs V_{CC}

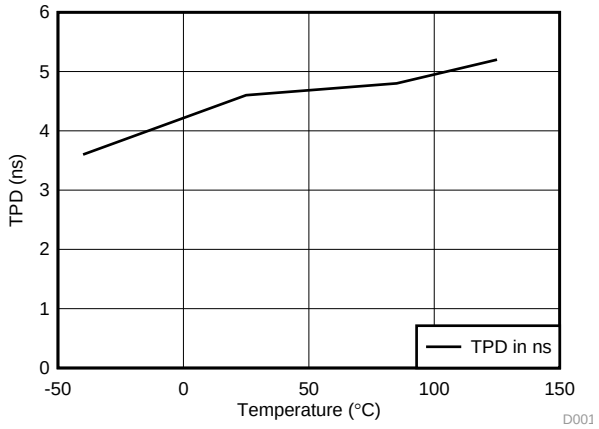
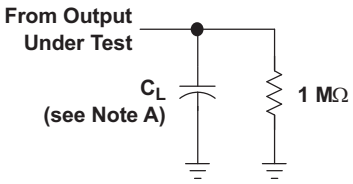


Figure 2. TPD vs Temperature

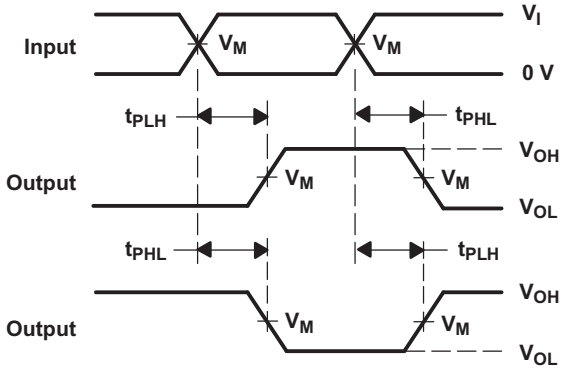
7 Parameter Measurement Information

7.1 Propagation Delays, Setup and Hold Times, and Pulse Width

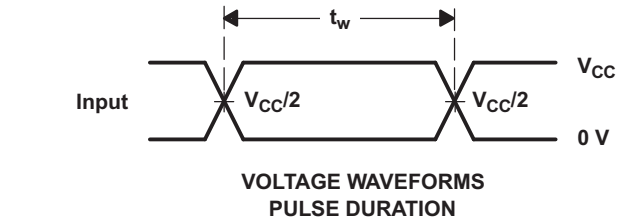


LOAD CIRCUIT

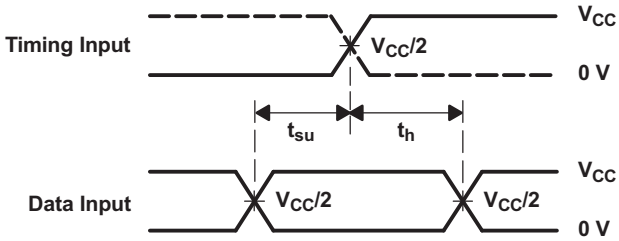
	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
PULSE DURATION

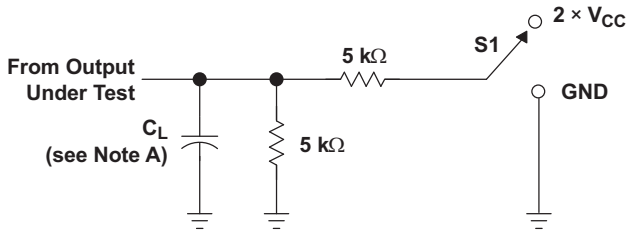


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

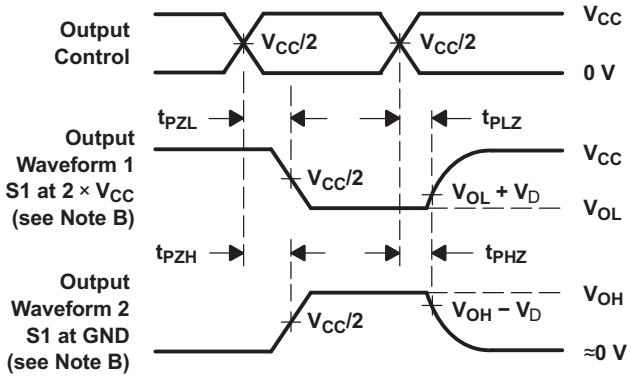
7.2 Enable and Disable Times



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	2 × V_{CC} GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_D	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74AUP1G79 is a single positive-edge-triggered D-type flip-flop. Data at the input (D) is transferred to the output (Q) on the positive-going edge of the clock pulse when the setup time requirement is met. Because the clock triggering occurs at a voltage level, it is not directly related to the rise time of the clock pulse. This allows for data at the input to be changed without affecting the level at the output, following the hold-time interval.

8.2 Functional Block Diagram

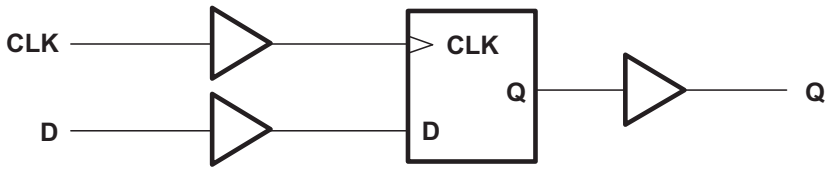


Figure 5. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined the in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modelled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics: T_A = 25°C*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics: T_A = 25°C*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by $\Delta t/\Delta v$ in *Recommended Operating Conditions* to avoid excessive currents and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Clamp Diodes

The inputs and outputs to this device have negative clamping diodes.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

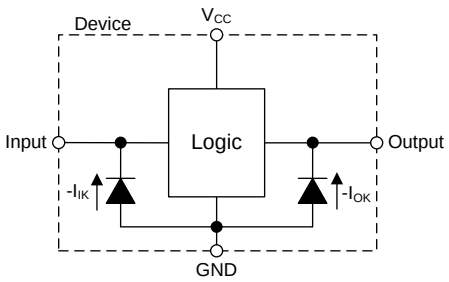


Figure 6. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics: T_A = 25°C*.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Absolute Maximum Ratings*.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74AUP1G79 device.

Table 1. Function Table

INPUTS		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L or H	X	Q_0

9 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A rotary quadrature encoder is a simple, infinitely-turning knob that outputs two out-of-phase square waves as it is turned and is often used in electronics as a method of human interface. One signal will lead the other in phase depending on which direction the knob is turned. The SN74AUP1G79 can be used to determine which direction the knob is being turned without the need for a microcontroller or other complex monitoring system by connecting the outputs of the knob to the D and CLK inputs of the SN74AUP1G79 as shown in Figure 7. It is important to note that the CLK input will control when the direction signal changes, as shown in Figure 8.

9.2 Typical Application

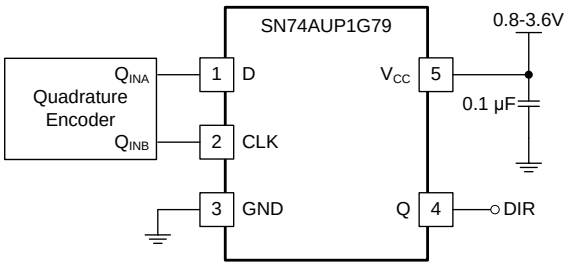


Figure 7. Typical Application Diagram

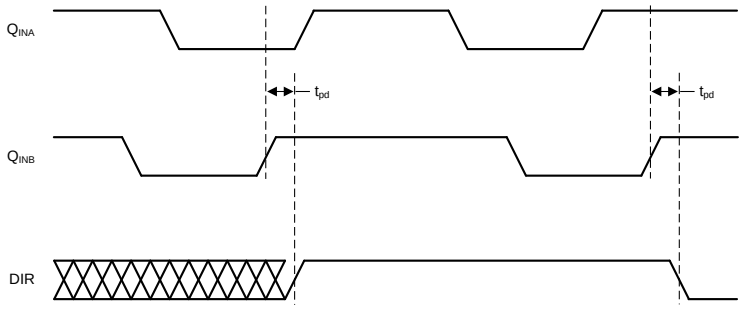


Figure 8. Timing Diagram for Quadrature Encoder Application

9.2.1 Design Requirements

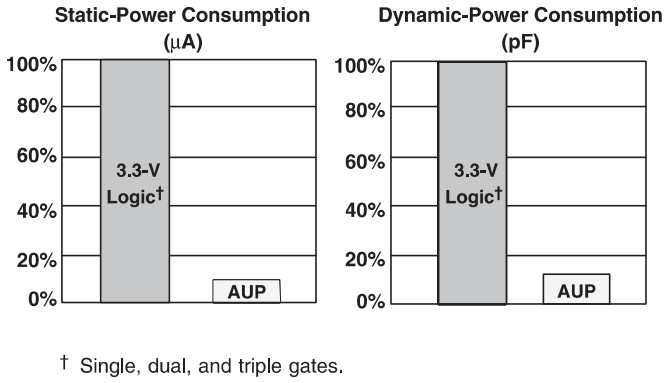
The SN74AUP1G79 device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

9.2.2 Detailed Design Procedure

1. Recommended Input conditions
   - Rise time and fall time specifications. See $\Delta t/\Delta V$ in *Recommended Operating Conditions*.
   - Specified high and low levels. See V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - Inputs are overvoltage tolerant, which allows them to go as high as 3.6 V at any valid V_{CC}
2. Recommended output conditions
   - Load currents must not exceed 20 mA on the output and 50 mA total for the part

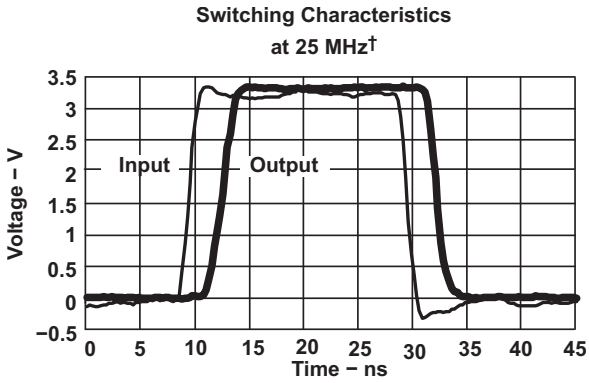
Typical Application (continued)

9.2.3 Application Curves



† Single, dual, and triple gates.

Figure 9. AUP – The Lowest-Power Family



† AUP1G08 data at C_L = 15 pF

Figure 10. Excellent Signal Integrity

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table. A 0.1-µF bypass capacitor is recommended to be connected from the VCC terminal to GND to prevent power disturbance. To reject different frequencies of noise, use multiple bypass capacitors in parallel. Capacitors with values of 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor must be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 11 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

An example layout is given in Figure 12 for the DPW (X2SON-5) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout

11.2 Layout Example

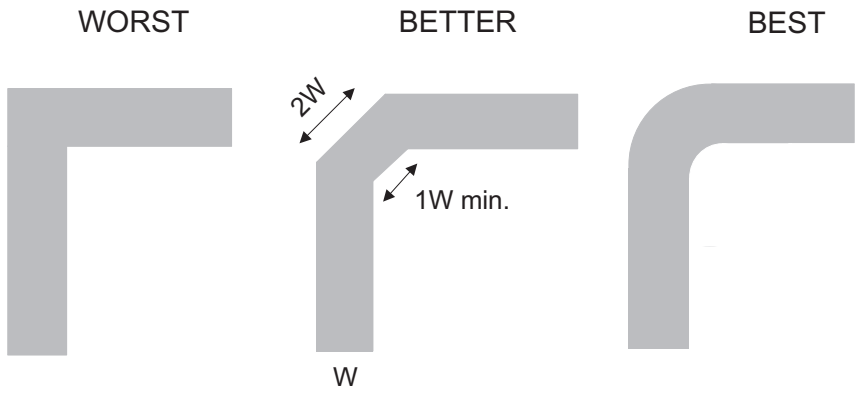


Figure 11. Trace Example

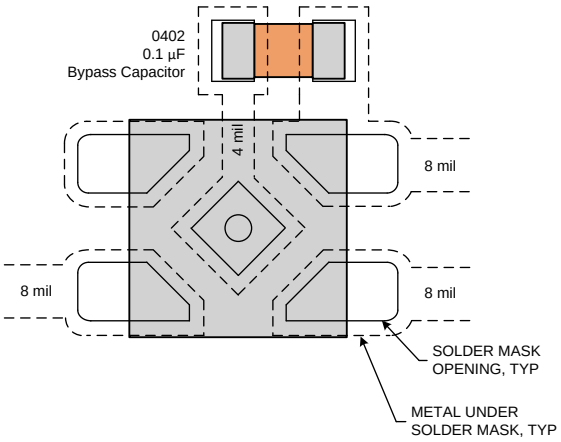


Figure 12. Example Layout With DPW (X2SON-5) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

NanoStar, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G79DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	H79R	Samples
SN74AUP1G79DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HWF, HWK, HWO, HWR)	Samples
SN74AUP1G79DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HWO, HWR)	Samples
SN74AUP1G79DPWR	ACTIVE	X2SON	DPW	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	9N	Samples
SN74AUP1G79DRLR	ACTIVE	SOT-5X3	DRL	5	4000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HWR	Samples
SN74AUP1G79DRYR	ACTIVE	SON	DRY	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HW	Samples
SN74AUP1G79DSFR	ACTIVE	SON	DSF	6	5000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HW	Samples
SN74AUP1G79YFPR	ACTIVE	DSBGA	YFP	6	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		HWN	Samples
SN74AUP1G79YZPR	ACTIVE	DSBGA	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HWN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

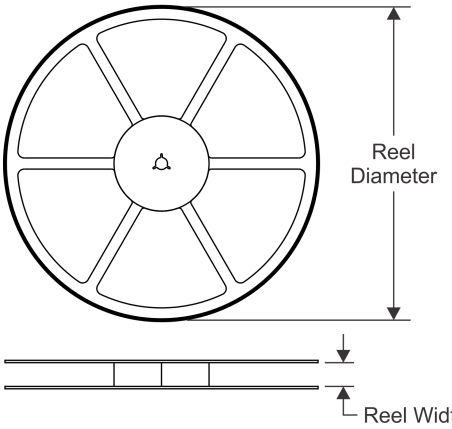
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

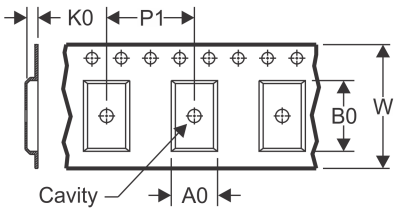
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

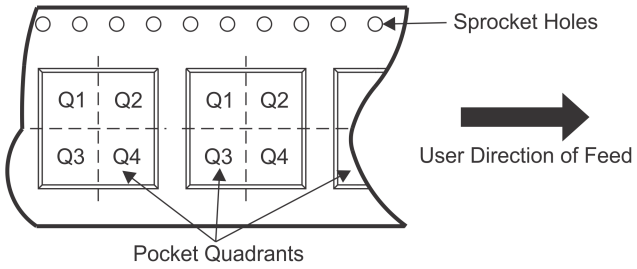


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

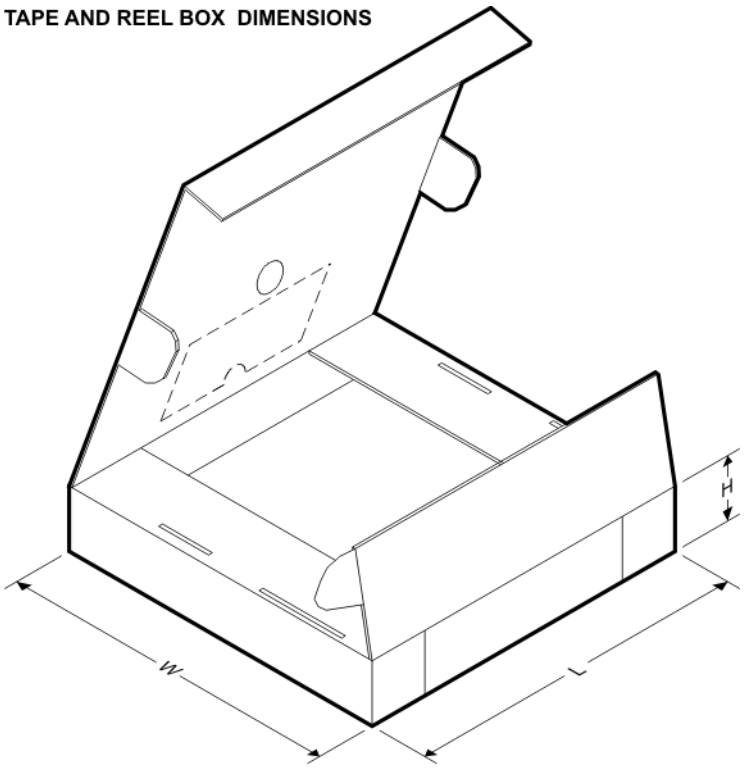
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G79DCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
SN74AUP1G79DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G79DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G79DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G79DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G79DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G79DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G79YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G79DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G79DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G79DCKR	SC70	DCK	5	3000	205.0	200.0	33.0
SN74AUP1G79DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G79DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G79DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G79DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G79DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G79DSFR	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G79YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G79YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

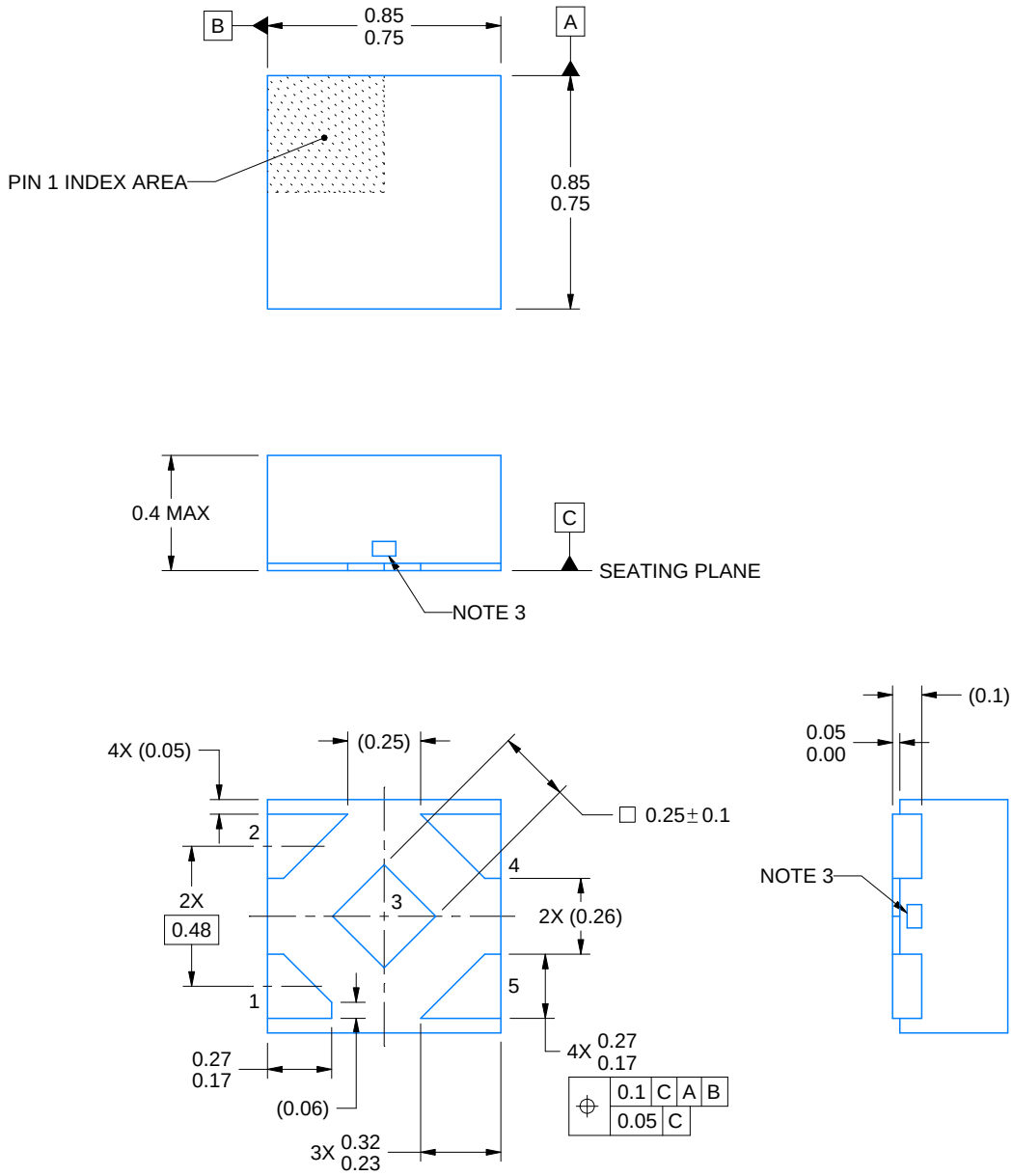
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

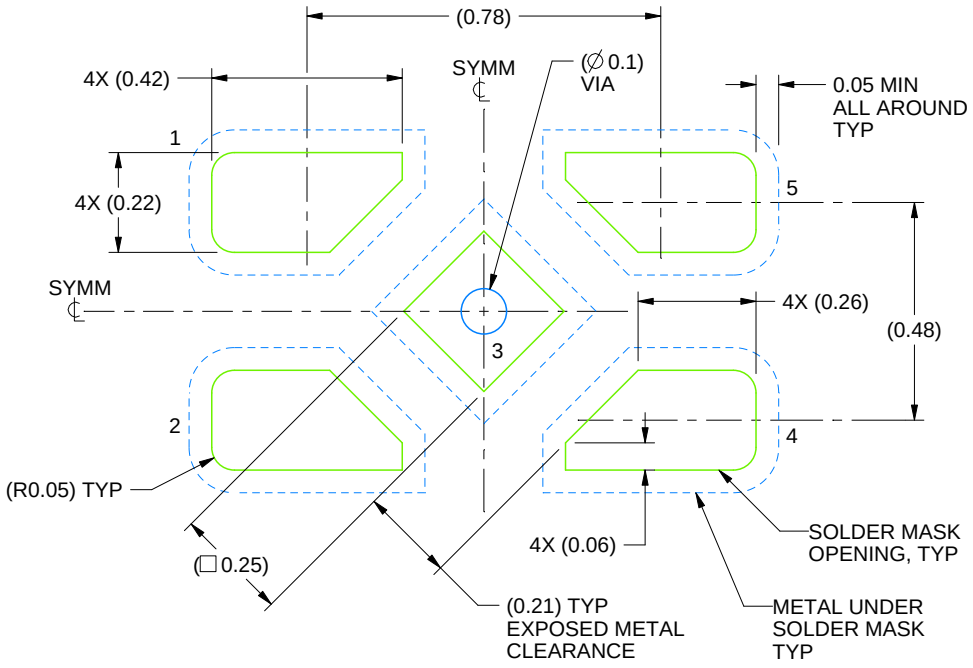
PLASTIC SMALL OUTLINE - NO LEAD



4223102/B 09/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

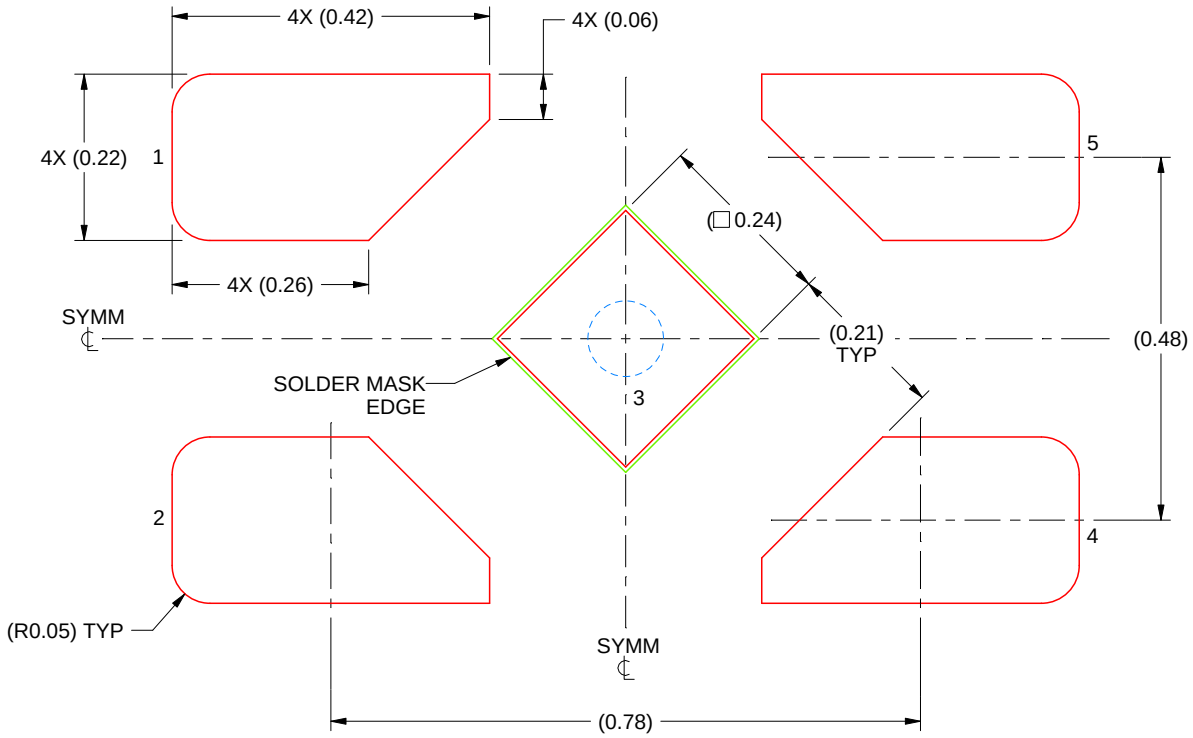


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/B 09/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

4223102/B 09/2017

NOTES: (continued)

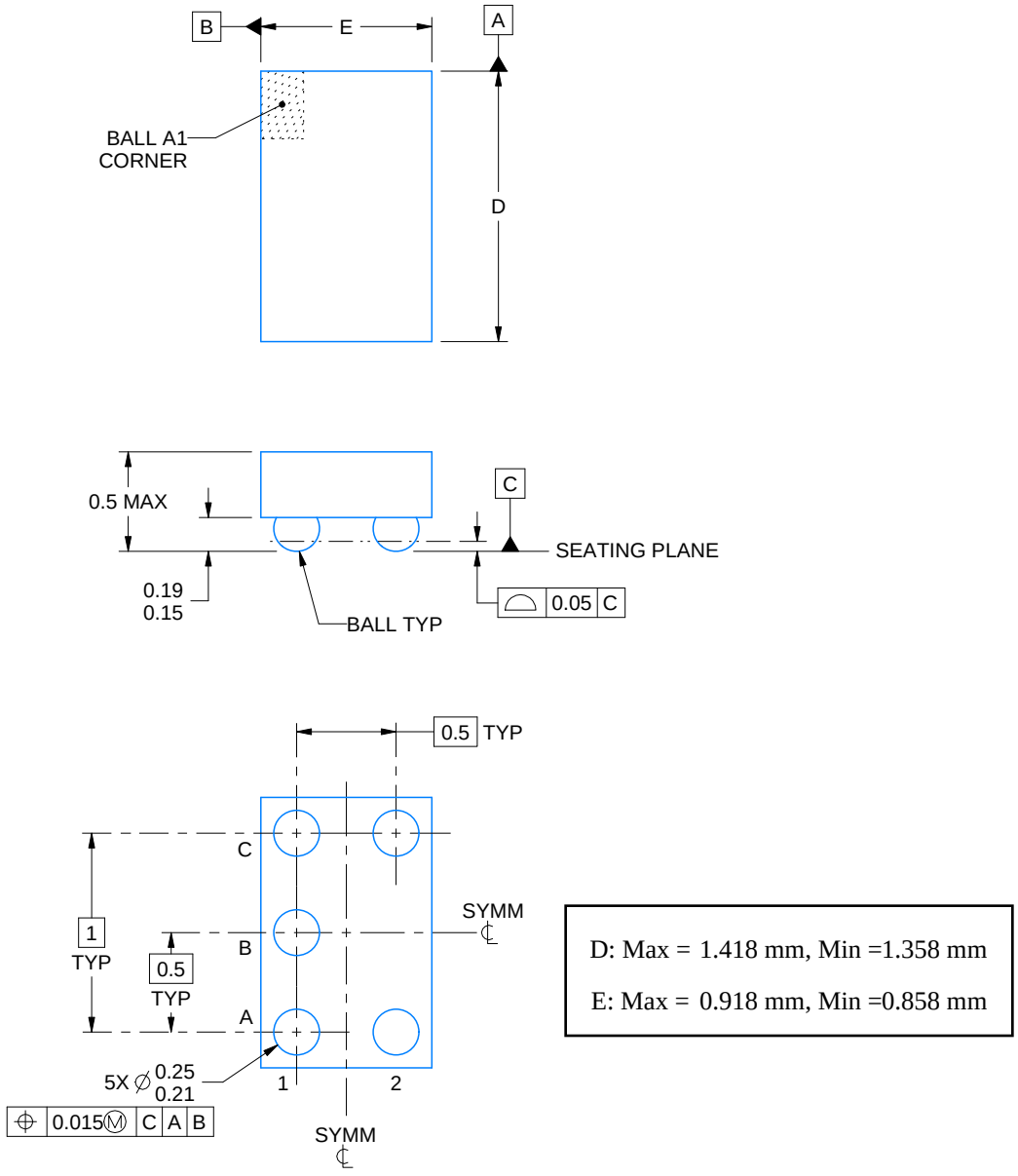
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



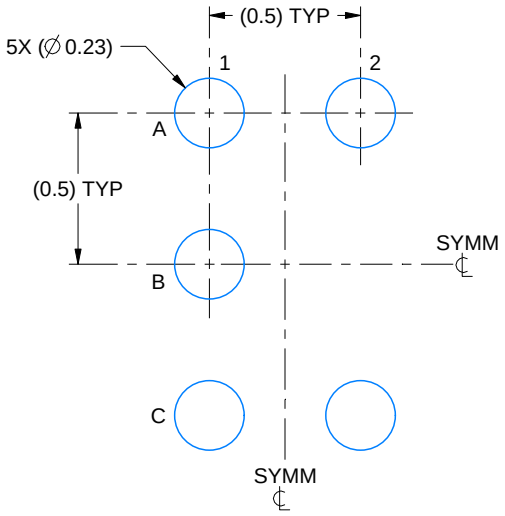
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

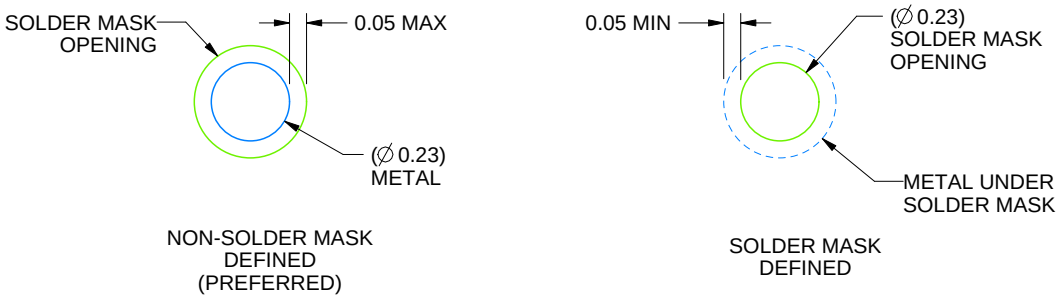
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

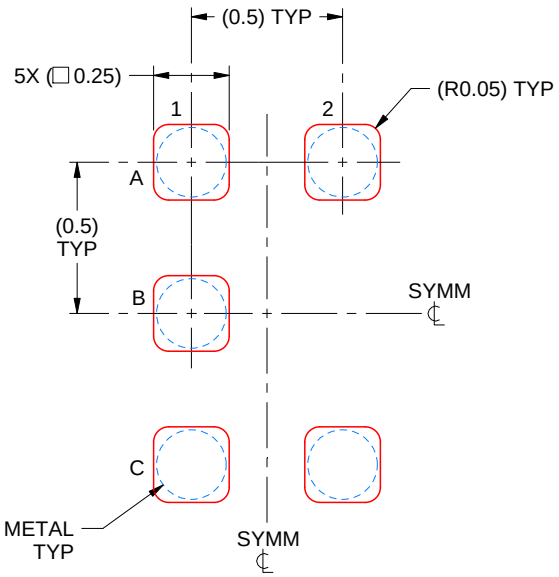


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

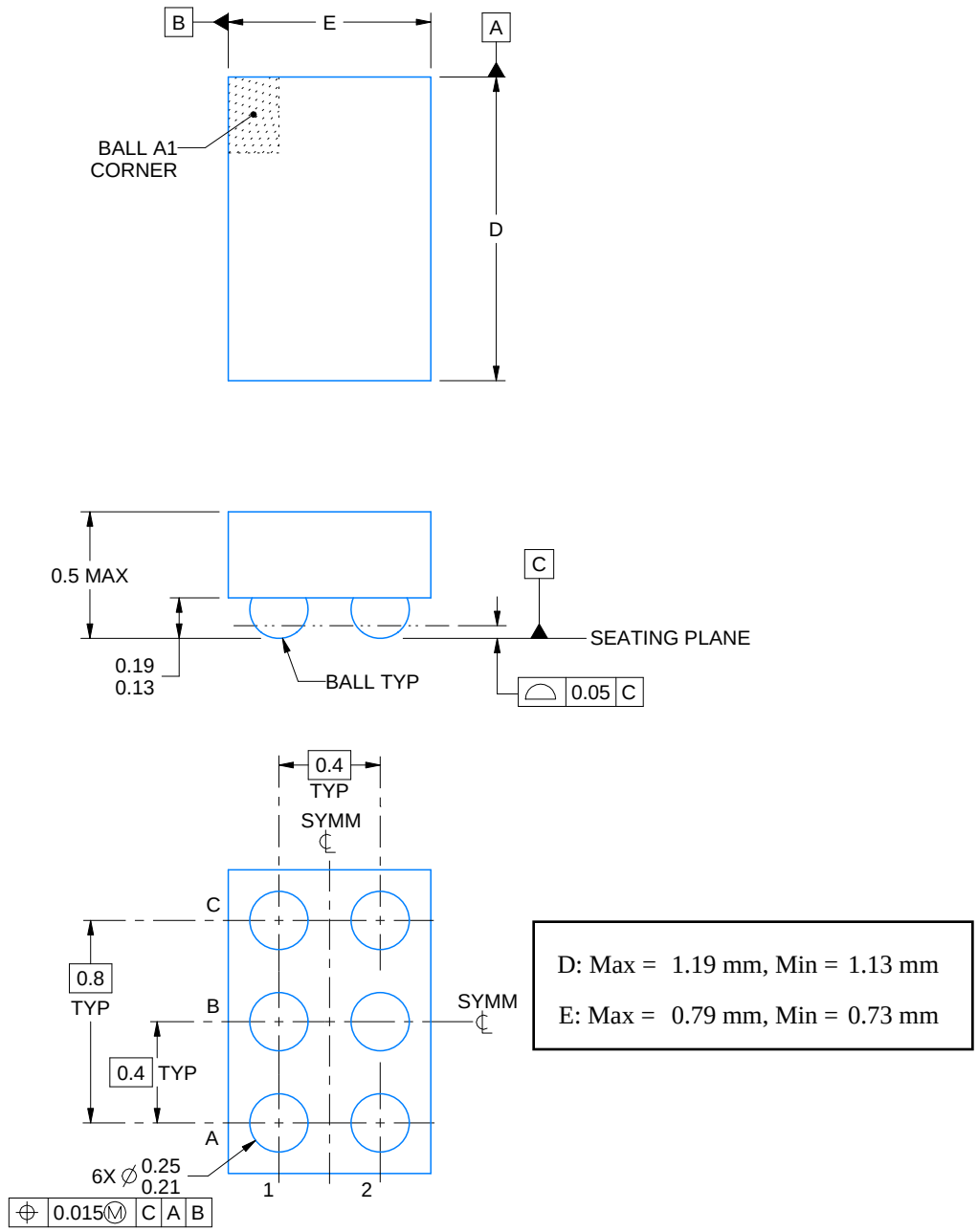
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

YFP0006

DSBGA - 0.5 mm max height

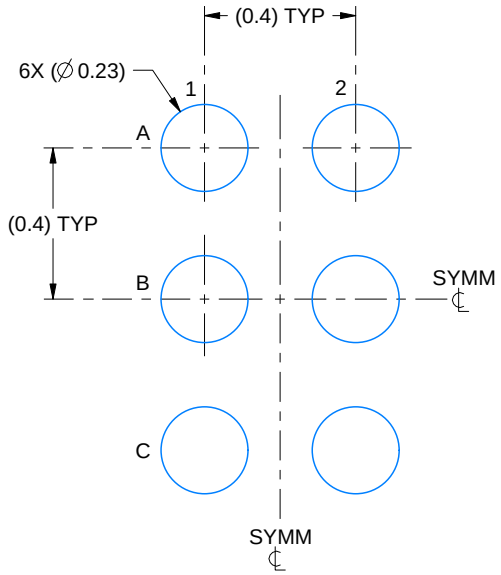
DIE SIZE BALL GRID ARRAY



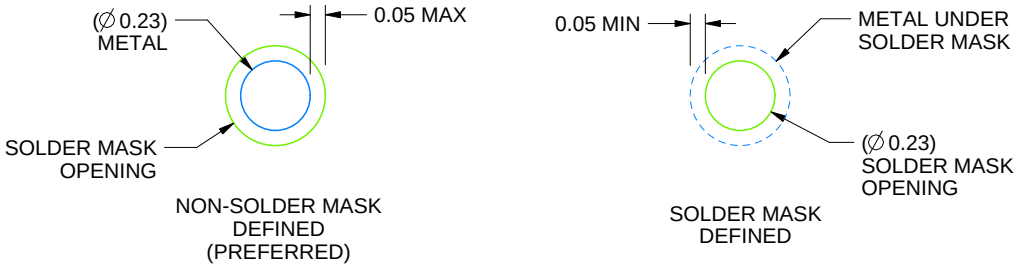
4223410/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

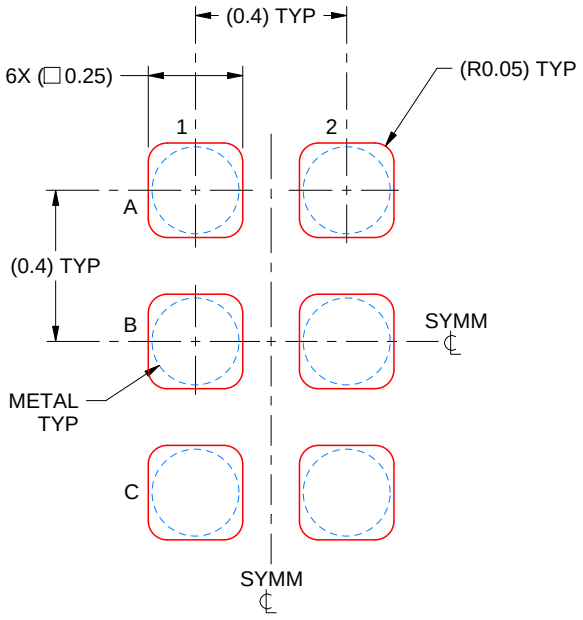


SOLDER MASK DETAILS
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

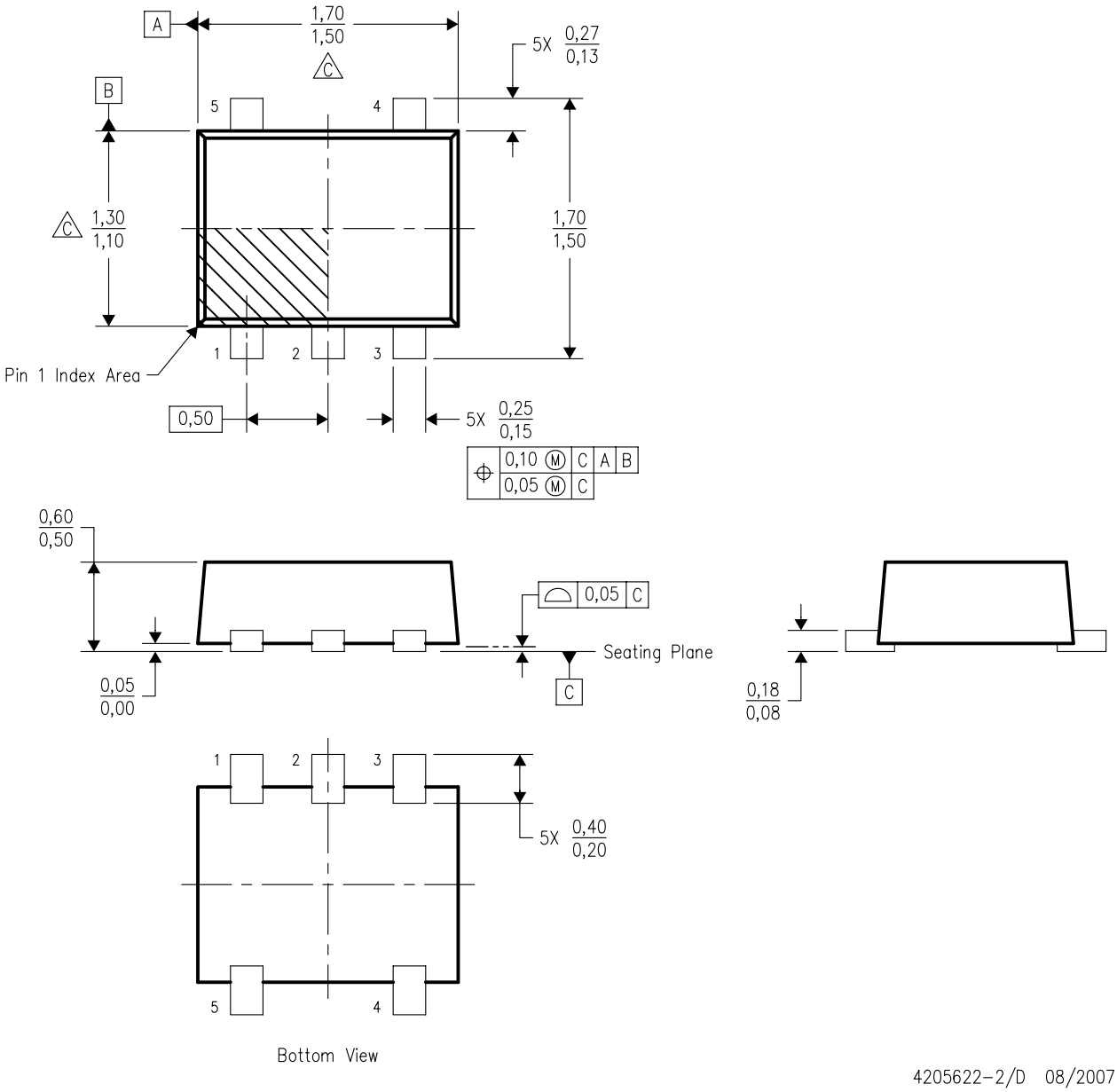


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

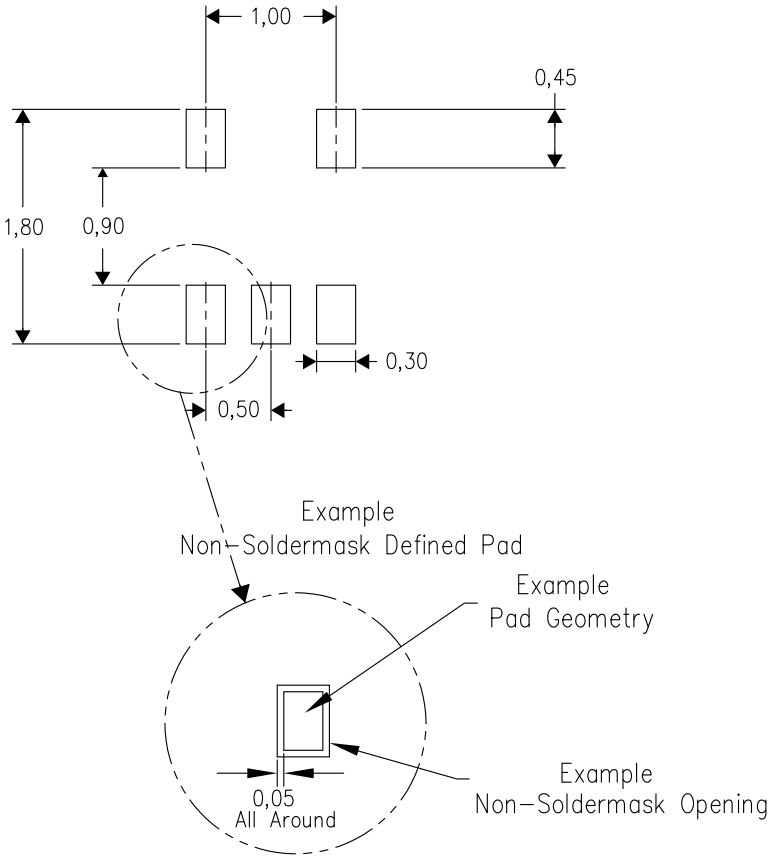
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



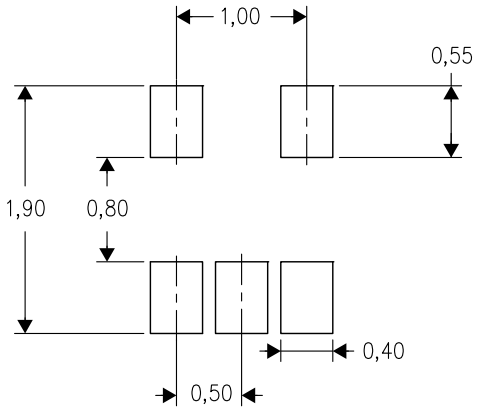
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
D. JEDEC package registration is pending.

DRL (R–PDSO–N5) PLASTIC SMALL OUTLINE

Example Board Layout



Example Stencil Design
(Note E)



4208207–2/E 06/12

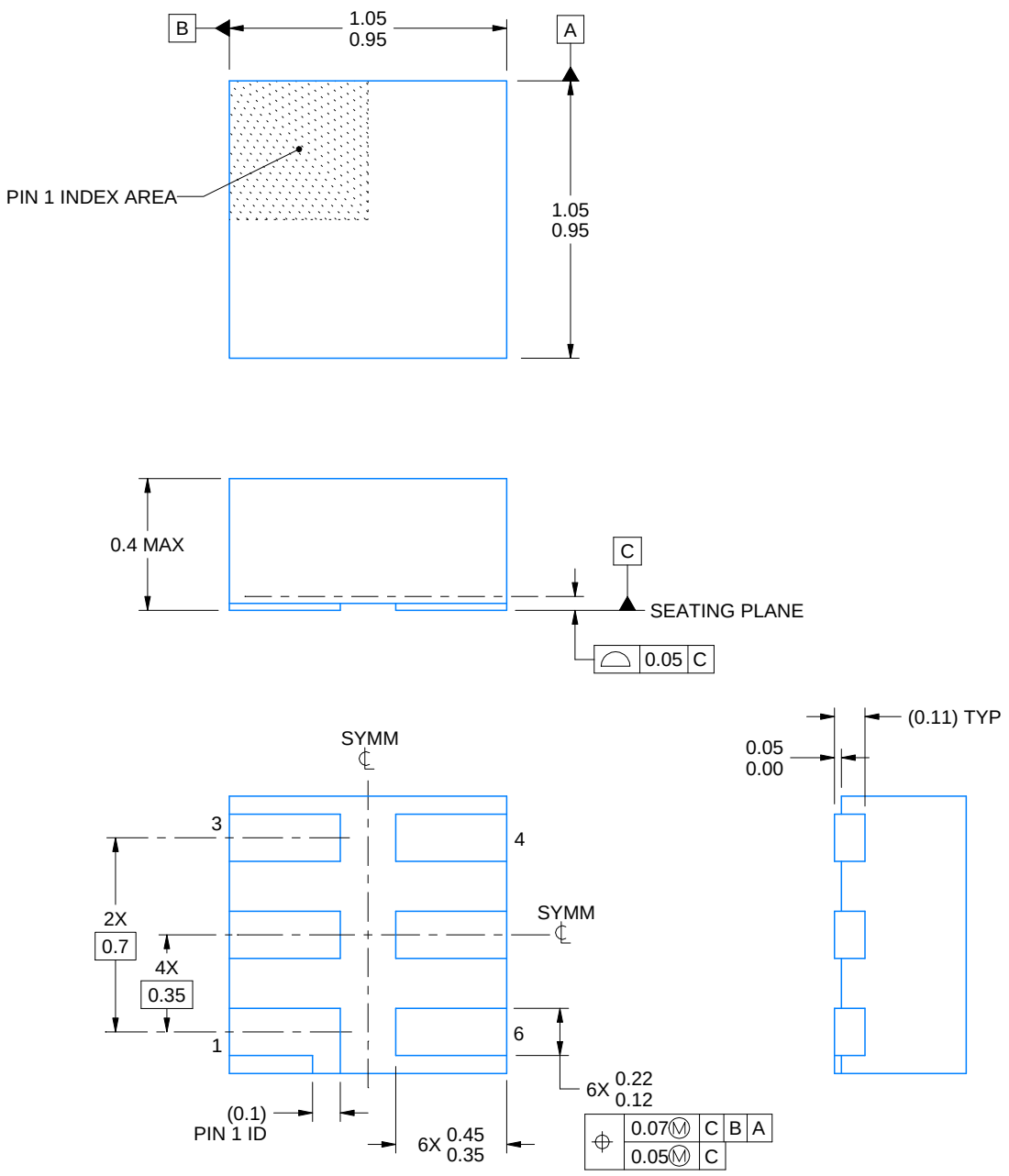
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

PACKAGE OUTLINE

DSF0006A

X2SON - 0.4 mm max height

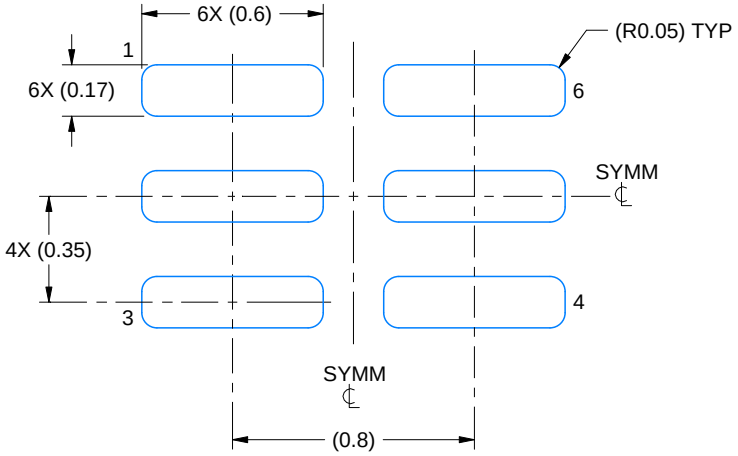
PLASTIC SMALL OUTLINE - NO LEAD



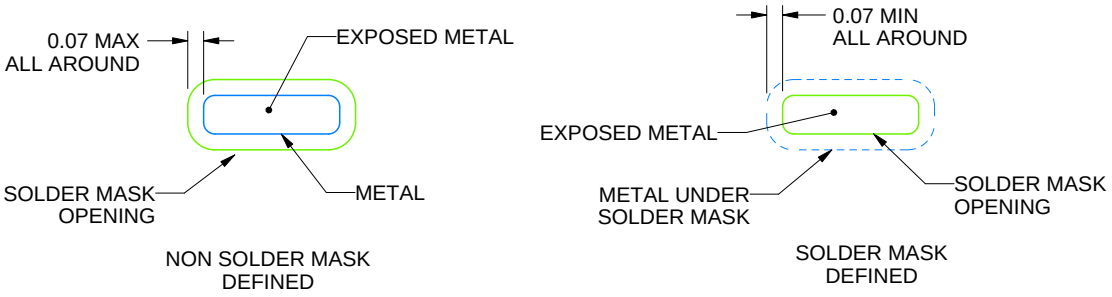
4220597/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220597/A 06/2017

NOTES: (continued)

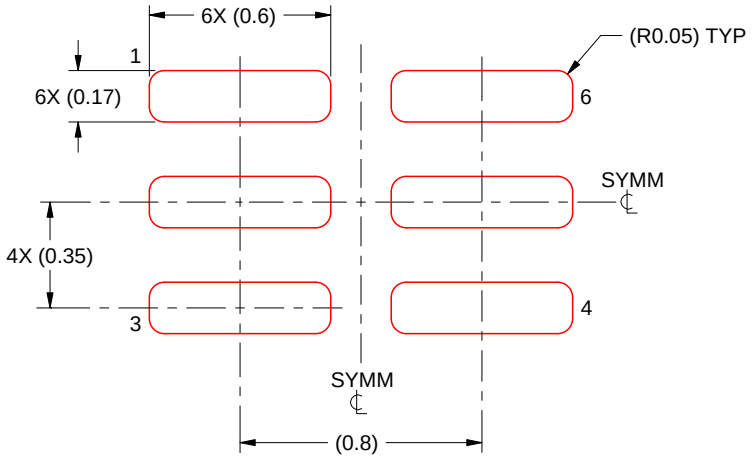
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



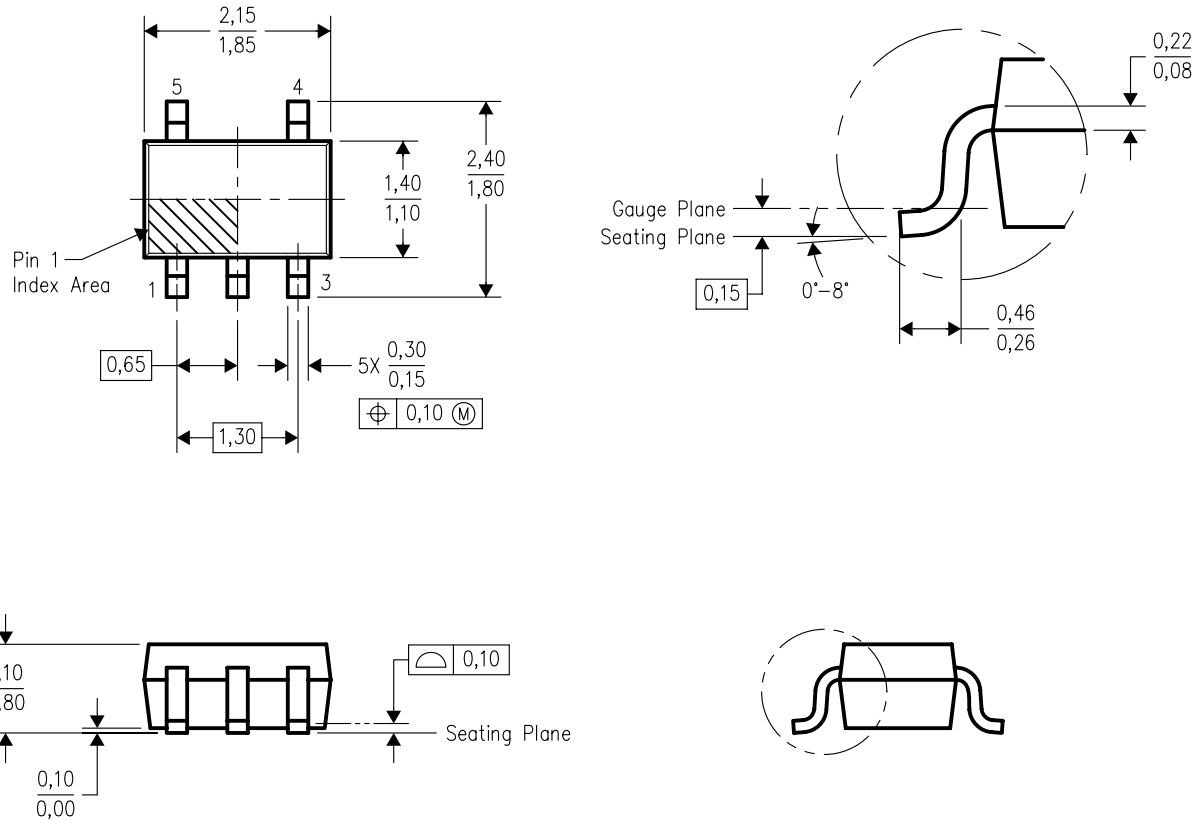
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

4220597/A 06/2017

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

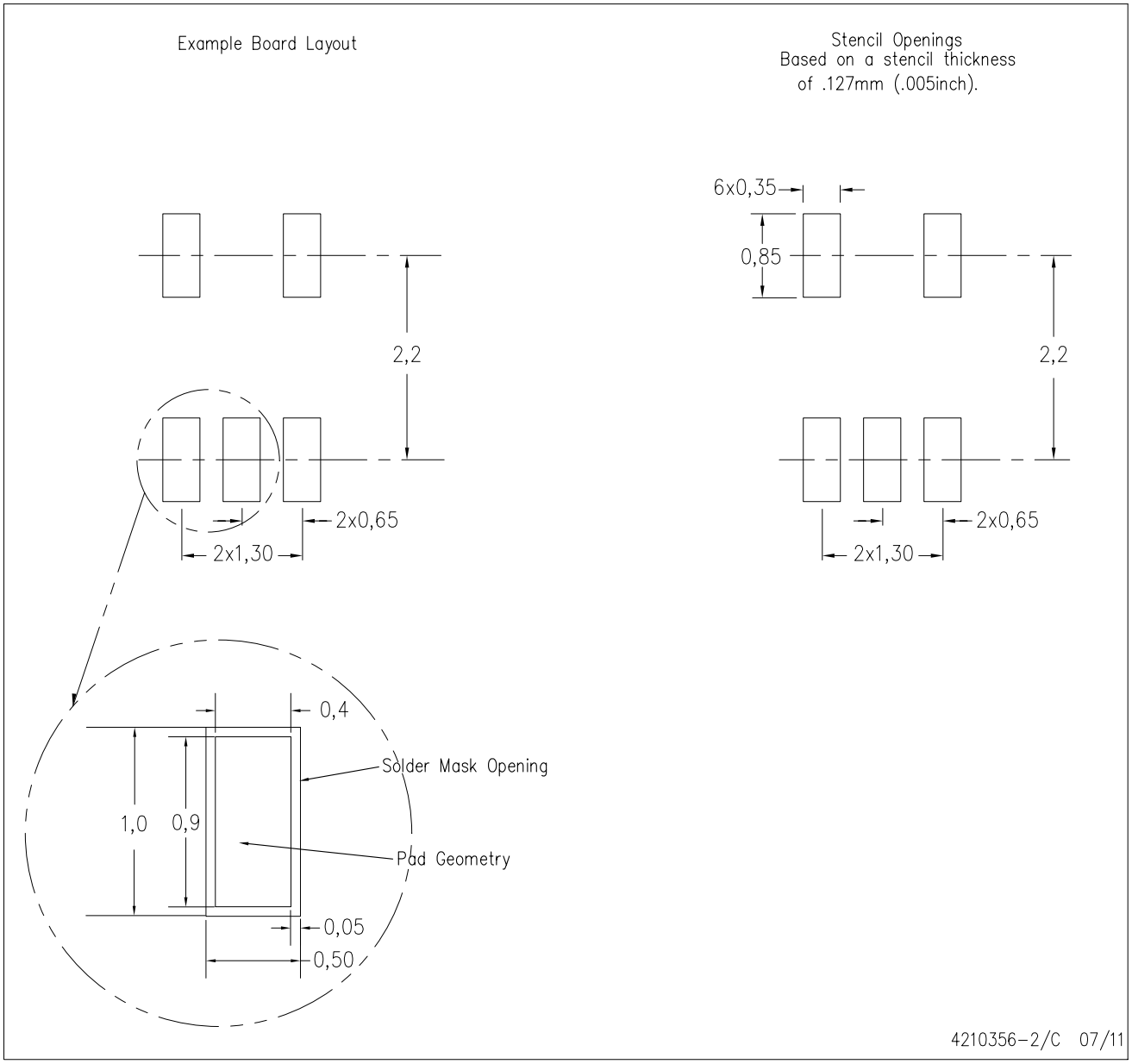
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



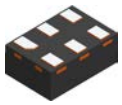
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

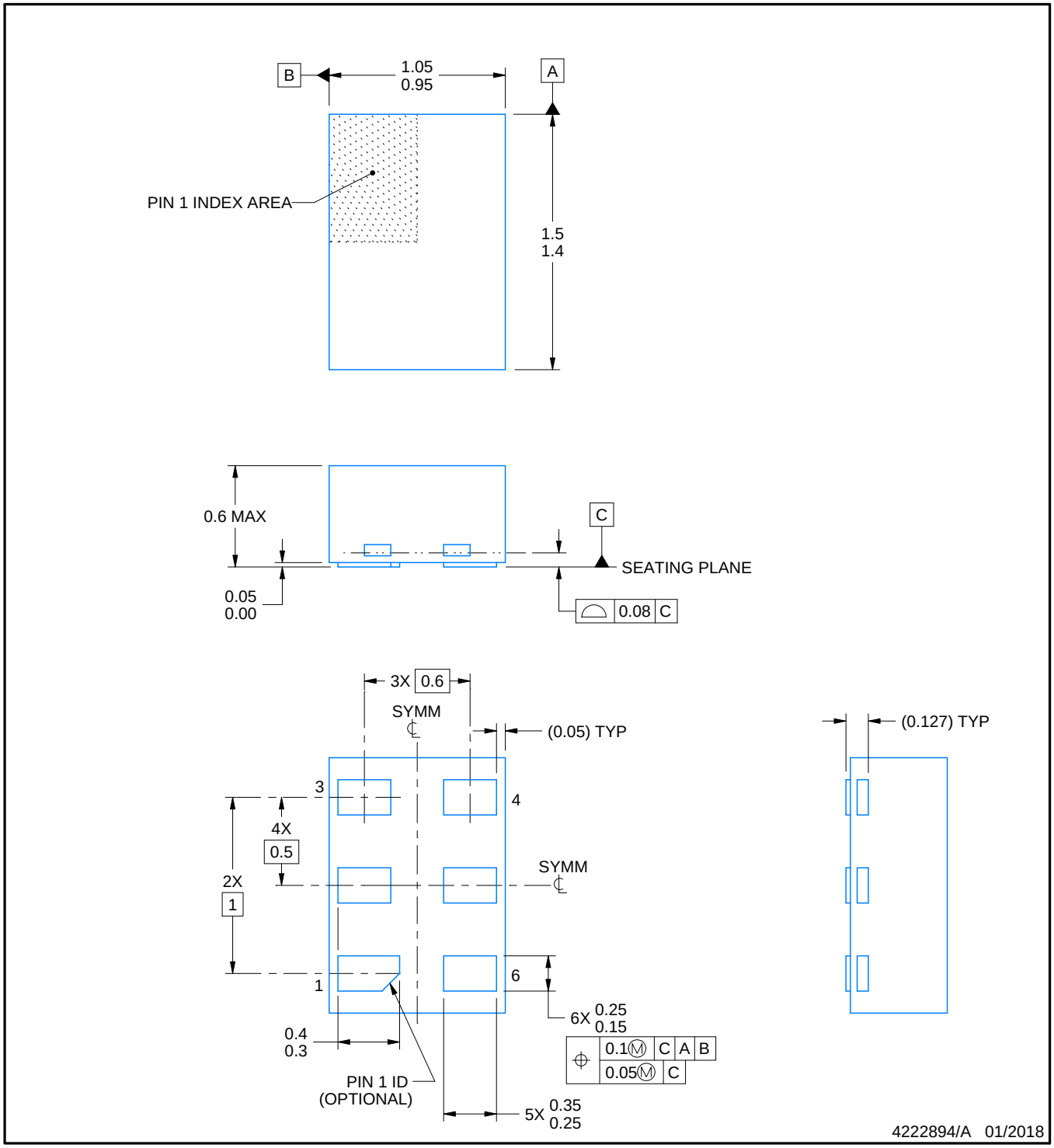
DRY0006A



PACKAGE OUTLINE

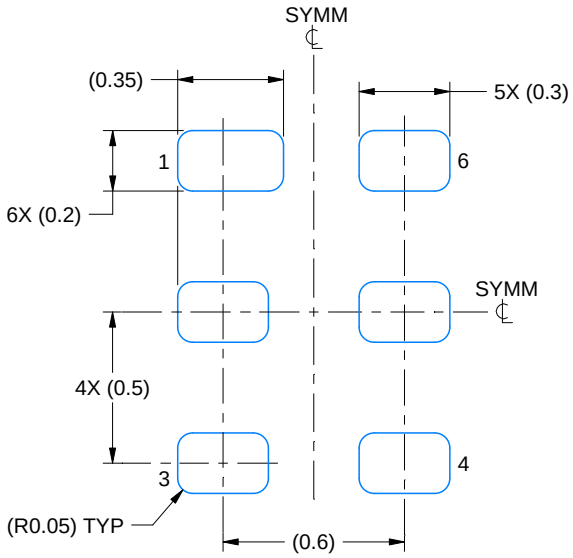
USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

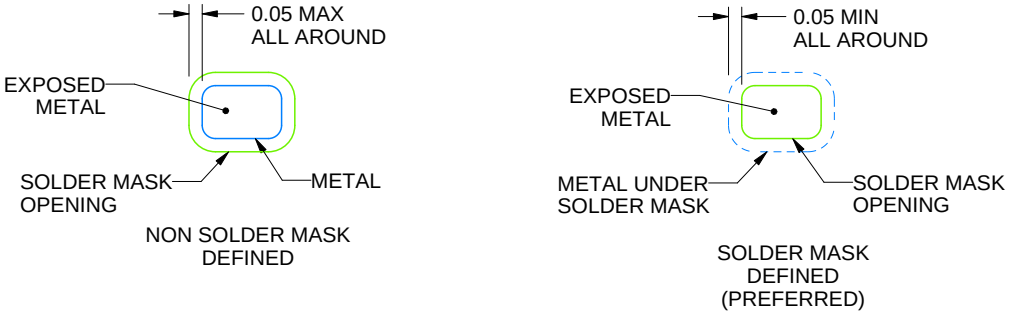


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

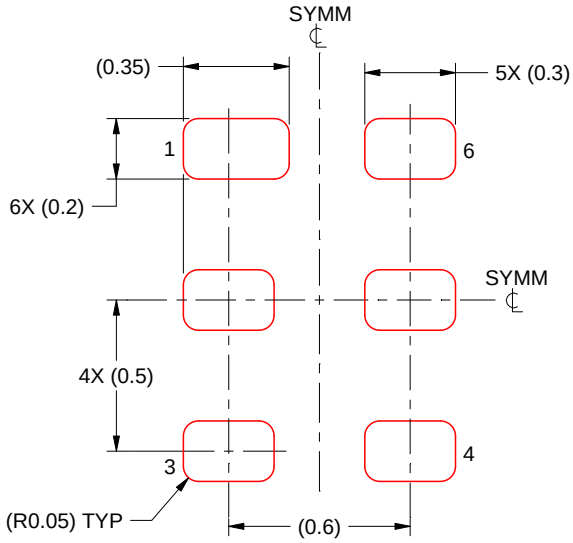
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

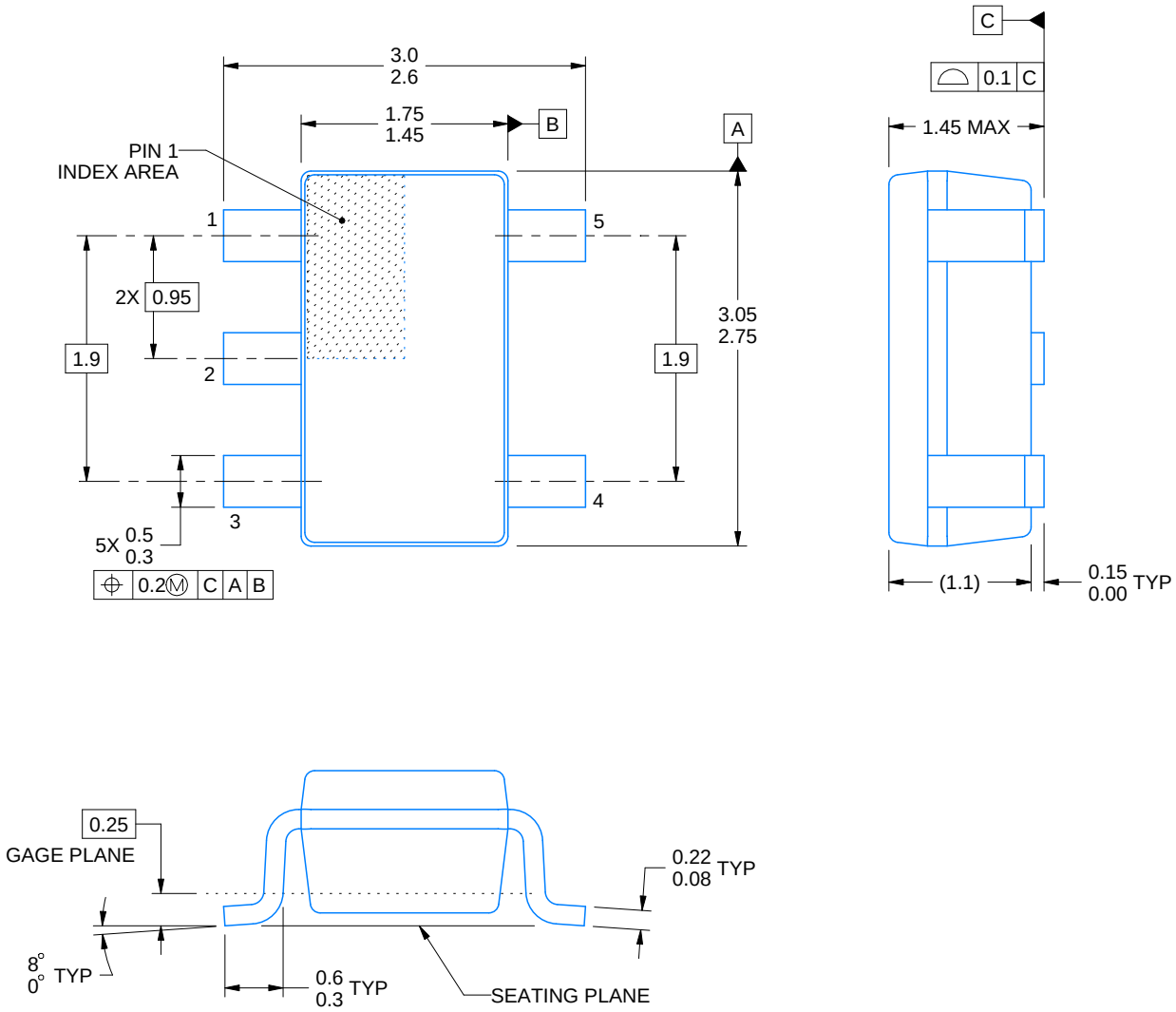
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

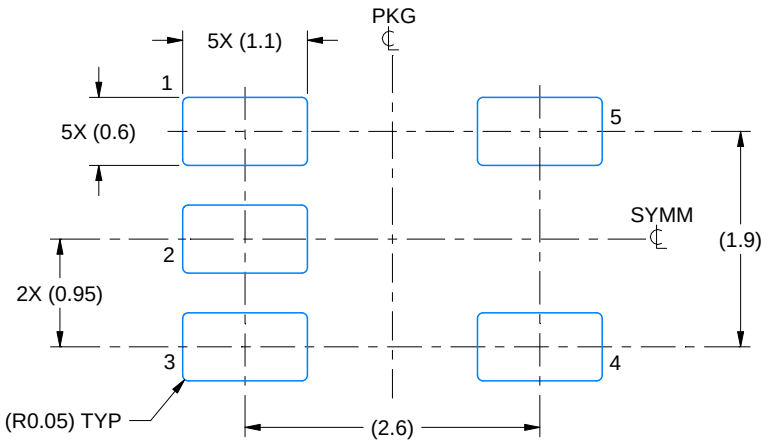
SMALL OUTLINE TRANSISTOR



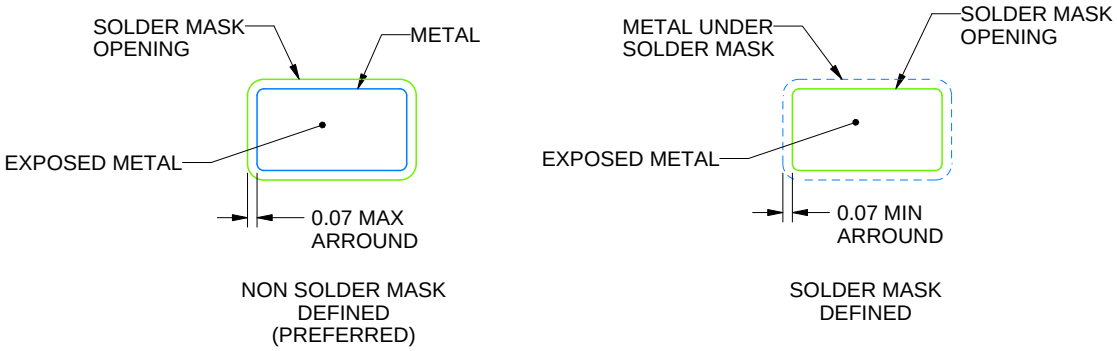
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

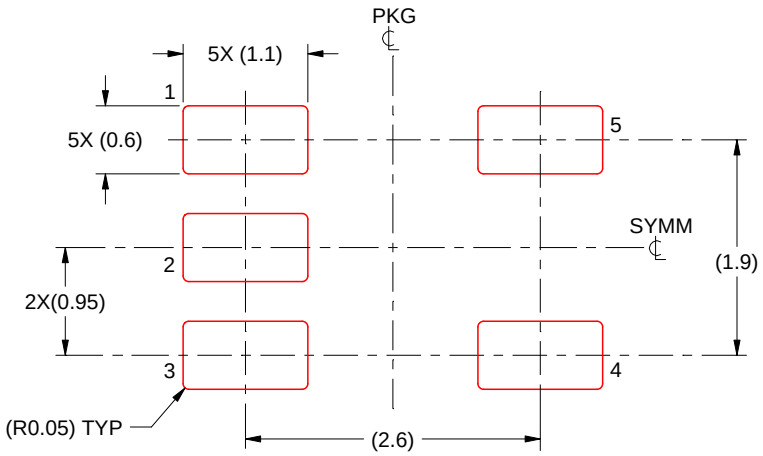


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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