LMV3xx Low-Voltage Rail-to-Rail Output Operational Amplifiers

1 Features

- 2.7-V and 5-V Performance
- –40°C to 125°C Operation
- Low-Power Shutdown Mode (LMV324S)
- No Crossover Distortion
- Low Supply Current
  - LMV321: 130 µA Typ
  - LMV358: 210 µA Typ
  - LMV324: 410 µA Typ
  - LMV324S: 410 µA Typ
- Rail-to-Rail Output Swing
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 1000-V Charged-Device Model

2 Applications

- Desktop PCs
- HVAC: Heating, Ventilating, and Air Conditioning
- Motor Control: AC Induction
- Netbooks
- Portable Media Players
- Power: Telecom DC/DC Module: Digital
- Pro Audio Mixers
- Refrigerators
- Washing Machines: High-End and Low-End

3 Description

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. These devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. With package sizes down to one-half the size of the DBV (SOT-23) package, these devices can be used for a variety of applications.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE
LMV324	SOIC (14)	8.65 mm × 3.91 mm
LMV321	SOT-23 (5)	2.90 mm × 1.60 mm
	SC-70 (5)	2.00 mm × 1.25 mm
LMV358	VSSOP (8)	2.30 mm × 2.00 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	TSSOP (8)	3.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic

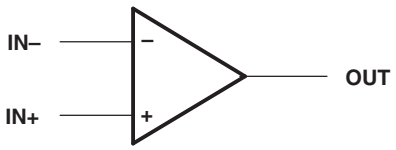


Table of Contents

5 Revision History

Changes from Revision V (December 2013) to Revision W **Page**

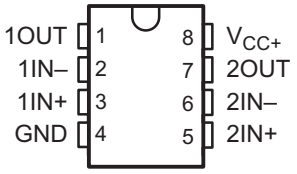
- Added Applications, Handling Rating table, Thermal Information Table, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section. ... 1

Changes from Revision U (July 2012) to Revision V **Page**

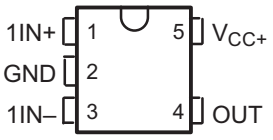
- Updated document to new TI data sheet format. ... 1
- Removed Ordering Information table. ... 3
- Added ESD warning. ... 23

6 Pin Configuration and Functions

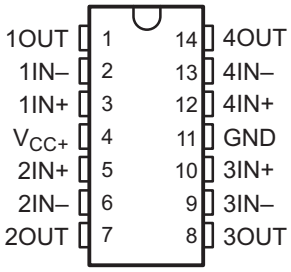
LMV358 . . . D (SOIC), DDU (VSSOP), DGK (VSSOP), OR PW (TSSOP) PACKAGE (TOP VIEW)



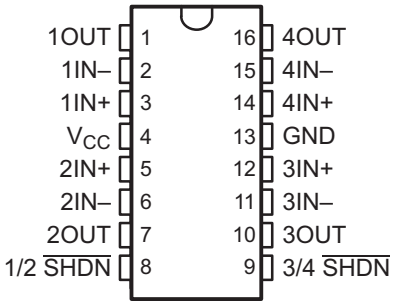
LMV321 . . . DBV (SOT-23) OR DCK (SC-70) PACKAGE (TOP VIEW)



LMV324 . . . D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



LMV324S . . . D (SOIC) OR PW (TSSOP) PACKAGE (TOP VIEW)



Pin Functions

PIN					TYPE	DESCRIPTION
NAME	LMV358	LMV321	LMV324	LMV324S		
	D, DDU, DGK, PW	DBV or DCK	D or PW	D or PW		
3/4 SHDN	—	—	—	9	I	Shutdown (logic low)/enable (logic high)
1/2 SHDN	—	—	—	8	I	Shutdown (logic low)/enable (logic high)
1IN+	3	1	3	3	I	Noninverting input
1IN–	2	3	2	2	I	Inverting input
2IN+	5	—	5	5	I	Noninverting input
2IN–	6	—	6	6	I	Inverting input
2OUT	7	—	7	7	O	Output
3IN+	—	—	10	12	I	Noninverting input
3IN–	—	—	9	11	I	Inverting input
3OUT	—	—	8	10	O	Output
4IN+	—	—	12	14	I	Noninverting input
4IN–	—	—	13	15	I	Inverting input
4OUT	—	—	14	16	O	Output
GND	4	2	11	13	-	Negative supply
OUT	1	4	1	1	O	OUT
VCC+	8	5	4	4	-	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (2)			5.5	V
V_{ID}	Differential input voltage (3)			±5.5	V
V_I	Input voltage range (either input)		–0.2	5.7	V
	Duration of output short circuit (one amplifier) to ground (4)	At or below T_A = 25°C, V_{CC} ≤ 5.5 V	Unlimited		
T_J	Operating virtual junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_{CC} specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	0	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (single-supply operation)		2.7	5.5	V
V_{IH}	Amplifier turn-on voltage level (LMV324S) (2)	V_{CC} = 2.7 V	1.7		V
		V_{CC} = 5 V	3.5		
V_{IL}	Amplifier turn-off voltage level (LMV324S)	V_{CC} = 2.7 V		0.7	V
		V_{CC} = 5 V		1.5	
T_A	Operating free-air temperature	I temperature (LMV321, LMV358, LMV324, LMV321IDCK)	–40	125	°C
		I temperature (LMV324S)	-40	85	
		Q temperature	–40	125	

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) V_{IH} should not be allowed to exceed V_{CC}.

7.4 Thermal Information

THERMAL METRIC (1)		LMV3xx										UNIT
		D			DBV	DCK	DDU	DGK	PW			
		8 PIN	14 PIN	16 PIN	5 PIN	5 PIN	8 PIN	8 PIN	8 PIN	14 PIN	16 PIN	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	86	73	206	252	210	172	149	113	108	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: V_{CC}+ = 2.7 V

V_{CC+} = 2.7 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IO}	Input offset voltage				1.7	7	mV
α_{VIO}	Average temperature coefficient of input offset voltage				5		µV/°C
I_{IB}	Input bias current				11	250	nA
I_{IO}	Input offset current				5	50	nA
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 1.7 V		50	63		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 2.7 V to 5 V, V_O = 1 V		50	60		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		0	–0.2		V
					1.9	1.7	
V_O	Output swing	R_L = 10 kΩ to 1.35 V	High level	V_{CC} – 100	V_{CC} – 10		mV
			Low level		60	180	
I_{CC}	Supply current	LMV321I			80	170	µA
		LMV358I (both amplifiers)			140	340	
		LMV324I and LMV324SI (all four amplifiers)			260	680	
B_1	Unity-gain bandwidth	C_L = 200 pF			1		MHz
Φ_m	Phase margin				60		deg
G_m	Gain margin				10		dB
V_n	Equivalent input noise voltage	f = 1 kHz			46		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.17		pA/√Hz

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.6 Electrical Characteristics: V_{CC}+ = 5 V

V_{CC+} = 5 V, at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A (1)	MIN	TYP(2)	MAX	UNIT
V_{IO}	Input offset voltage			25°C		1.7	7	mV
				Full range			9	
α_{VIO}	Average temperature coefficient of input offset voltage			25°C		5		µV/°C
I_{IB}	Input bias current			25°C		15	250	nA
				Full range			500	
I_{IO}	Input offset current			25°C		5	50	nA
				Full range			150	
CMRR	Common-mode rejection ratio	V_{CM} = 0 to 4 V		25°C	50	65		dB
k_{SVR}	Supply-voltage rejection ratio	V_{CC} = 2.7 V to 5 V, V_O = 1 V, V_{CM} = 1 V		25°C	50	60		dB
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2		V
						4.2	4	
V_O	Output swing	R_L = 2 kΩ to 2.5 V	High level	25°C	V_{CC} – 300	V_{CC} – 40		mV
				Full range	V_{CC} – 400			
			Low level	25°C		120	300	
				Full range			400	
		R_L = 10 kΩ to 2.5 V	High level	25°C	V_{CC} – 100	V_{CC} – 10		
				Full range	V_{CC} – 200			
			Low level	25°C		65	180	
				Full range			280	
A_{VD}	Large-signal differential voltage gain	R_L = 2 kΩ		25°C	15	100		V/mV
				Full range	10			
I_{OS}	Output short-circuit current	Sourcing, V_O = 0 V		25°C	5	60		mA
		Sinking, V_O = 5 V			10	160		
I_{CC}	Supply current	LMV321I		25°C		130	250	µA
				Full range			350	
		LMV358I (both amplifiers)		25°C		210	440	
				Full range			615	
		LMV324I and LMV324SI (all four amplifiers)		25°C		410	830	
				Full range			1160	
B_1	Unity-gain bandwidth	C_L = 200 pF		25°C		1		MHz
Φ_m	Phase margin			25°C		60		deg
G_m	Gain margin			25°C		10		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.21		pA/√Hz
SR	Slew rate			25°C		1		V/µs

(1) Full range T_A = –40°C to 125°C for I temperature(LMV321, LMV358, LMV324, LMV321IDCK), –40°C to 85°C for (LMV324S) and –40°C to 125°C for Q temperature.
(2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.7 Shutdown Characteristics, LMV324S: V_{CC}+ = 2.7 V

V_{CC+} = 2.7 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V			5	µA
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = Open (measured at 50% point)		2		µs
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = Open (measured at 50% point)		40		ns

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.8 Shutdown Characteristics, LMV324S: V_{CC}+ = 5 V

V_{CC+} = 5 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode (per channel)	$\overline{SHDN}$ ≤ 0.6 V, T_A = Full Temperature Range			5	µA
$t_{(on)}$	Amplifier turn-on time	A_V = 1, R_L = Open (measured at 50% point)		2		µs
$t_{(off)}$	Amplifier turn-off time	A_V = 1, R_L = Open (measured at 50% point)		40		ns

(1) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.

7.9 Typical Characteristics

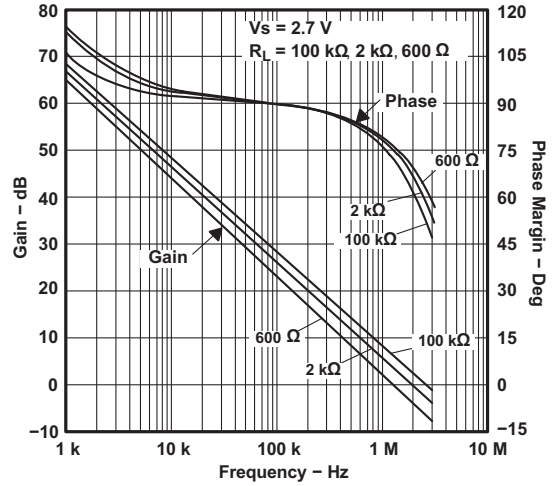


Figure 1. LMV321 Frequency Response vs Resistive Load

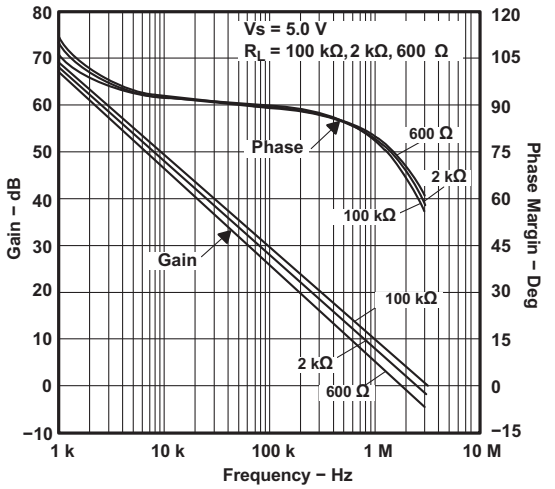


Figure 2. LMV321 Frequency Response vs Resistive Load

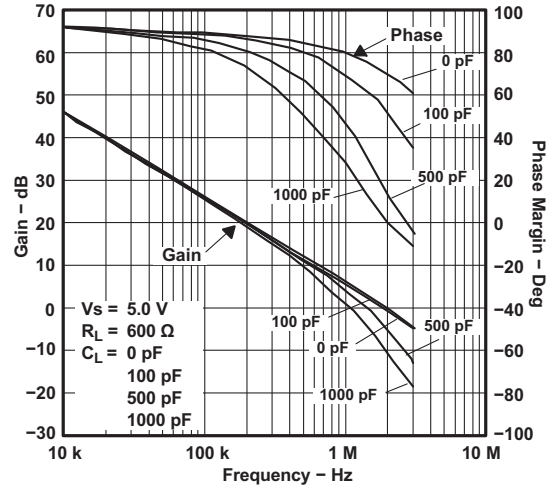


Figure 3. LMV321 Frequency Response vs Capacitive Load

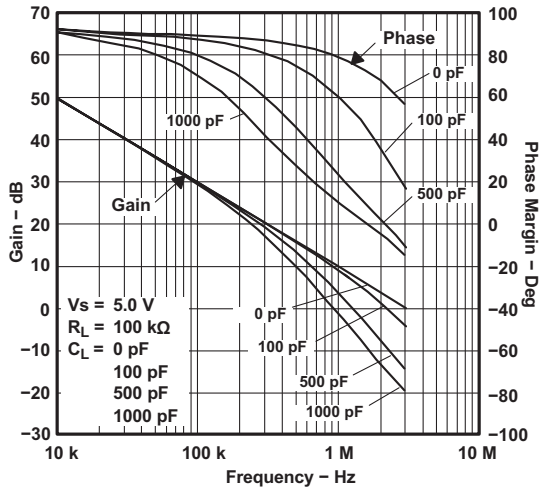


Figure 4. LMV321 Frequency Response vs Capacitive Load

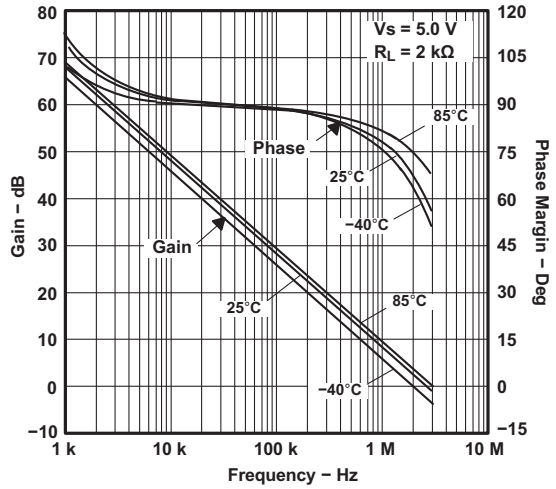


Figure 5. LMV321 Frequency Response vs Temperature

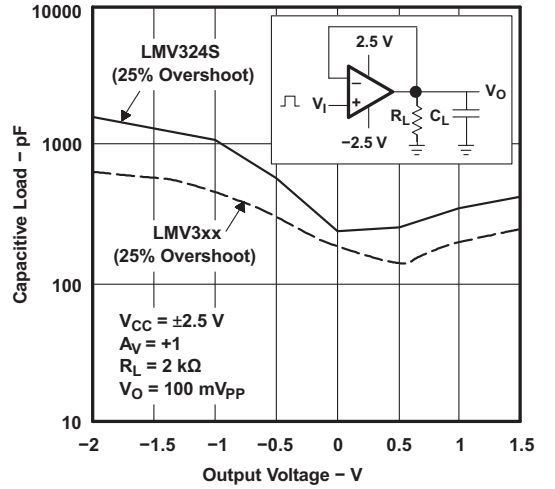


Figure 6. Stability vs Capacitive Load

Typical Characteristics (continued)

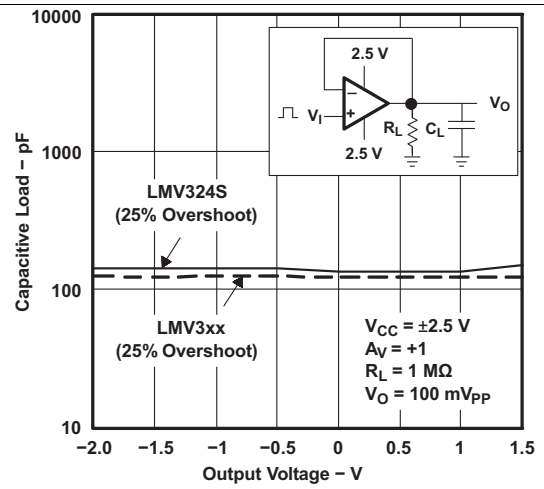


Figure 7. Stability vs Capacitive Load

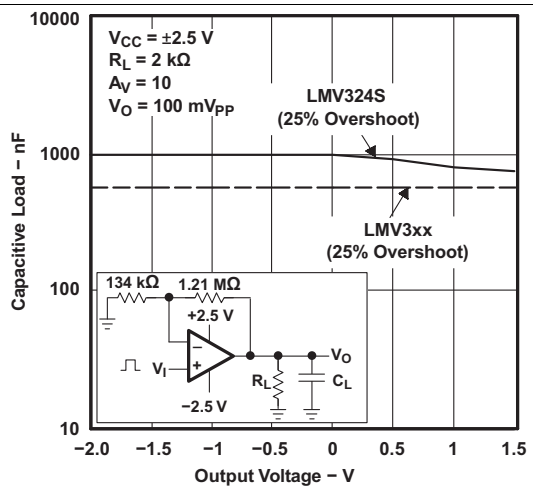


Figure 8. Stability vs Capacitive Load

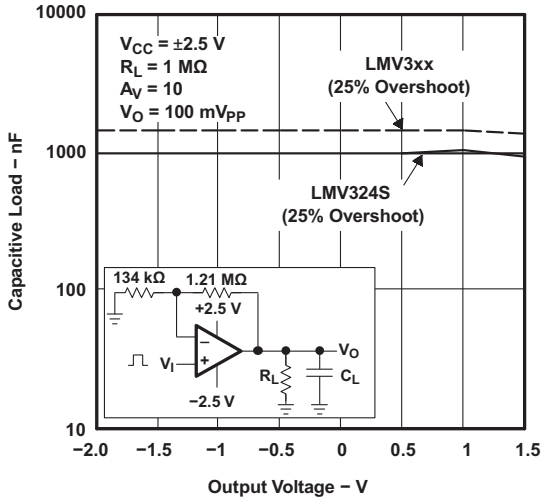


Figure 9. Stability vs Capacitive Load

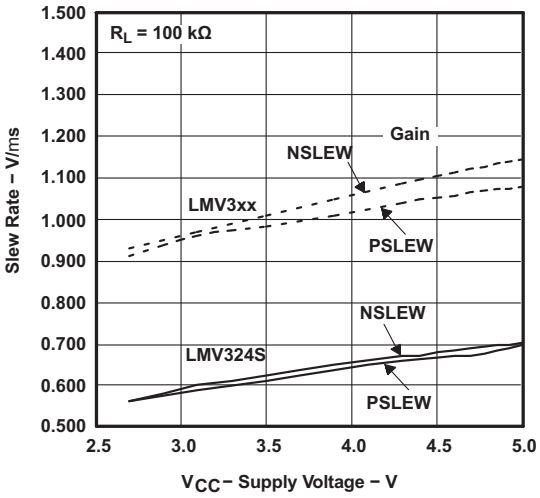


Figure 10. Slew Rate vs Supply Voltage

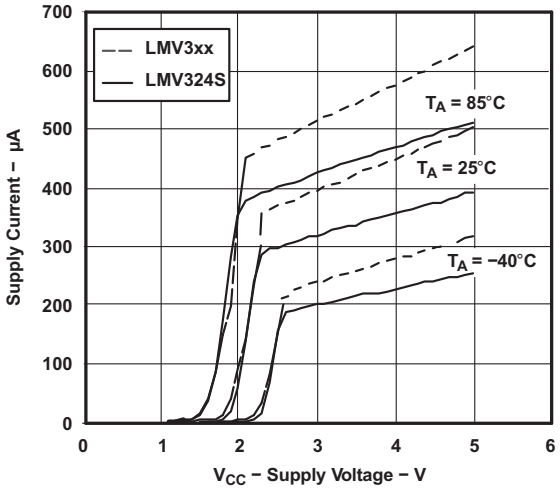


Figure 11. Supply Current vs Supply Voltage - Quad Amplifier

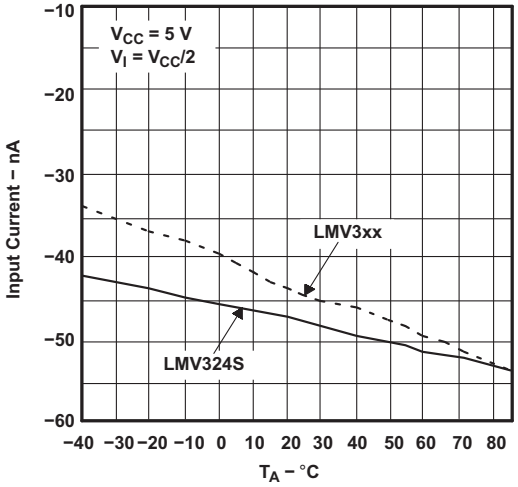


Figure 12. Input Current vs Temperature

Typical Characteristics (continued)

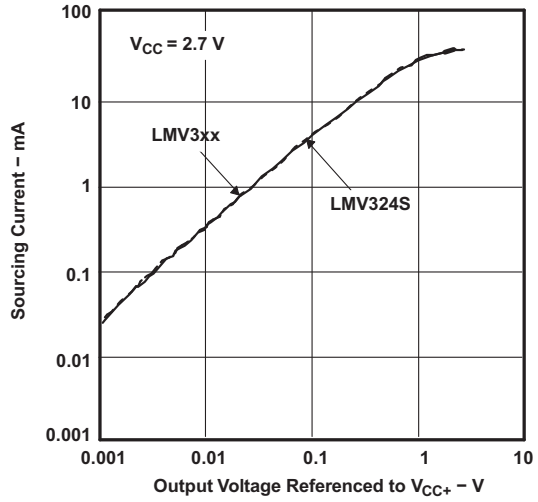


Figure 13. Source Current vs Output Voltage

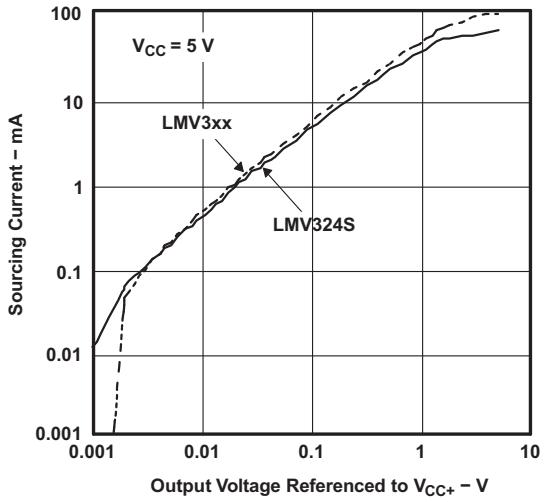


Figure 14. Source Current vs Output Voltage

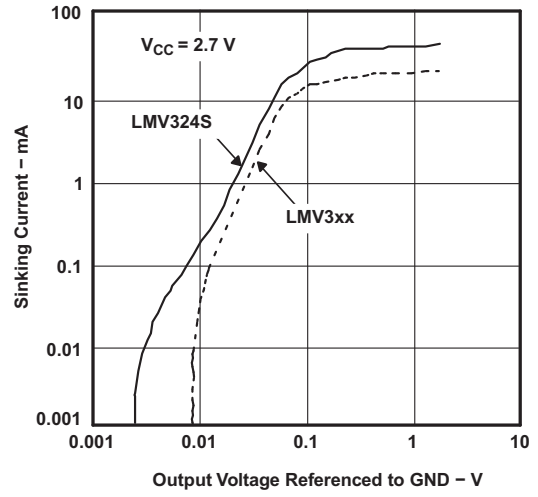


Figure 15. Sinking Current vs Output Voltage

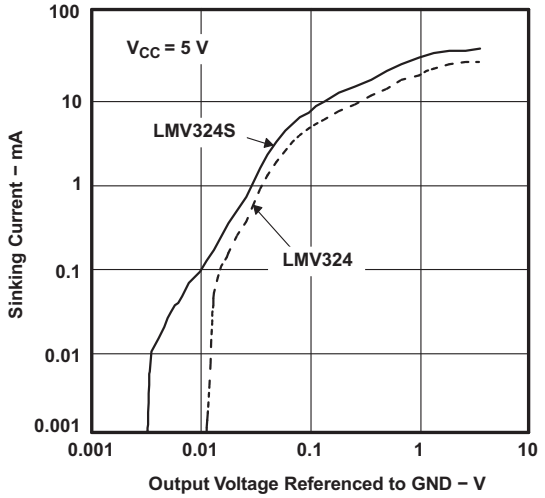


Figure 16. Sinking Current vs Output Voltage

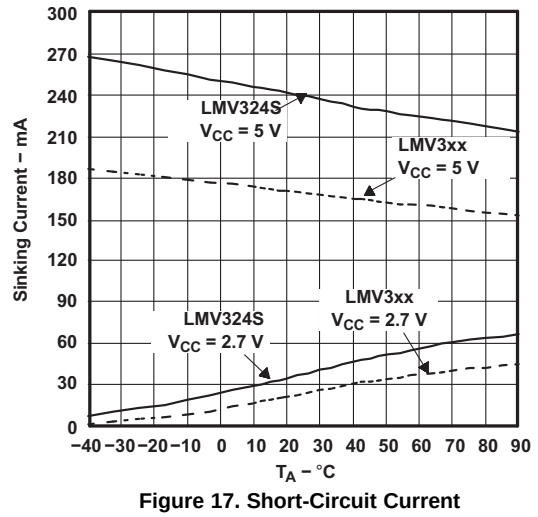


Figure 17. Short-Circuit Current vs Temperature

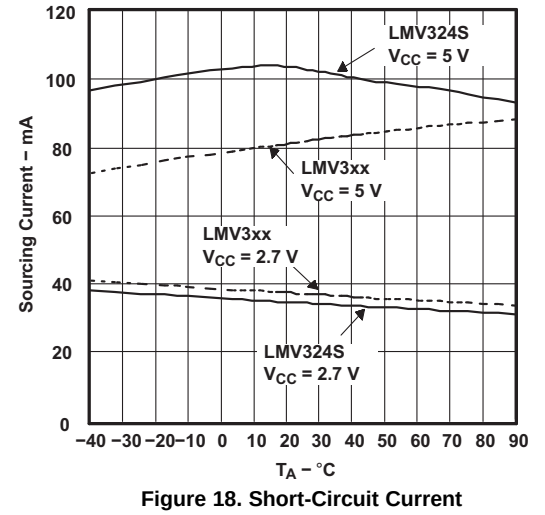


Figure 18. Short-Circuit Current vs Temperature

Typical Characteristics (continued)

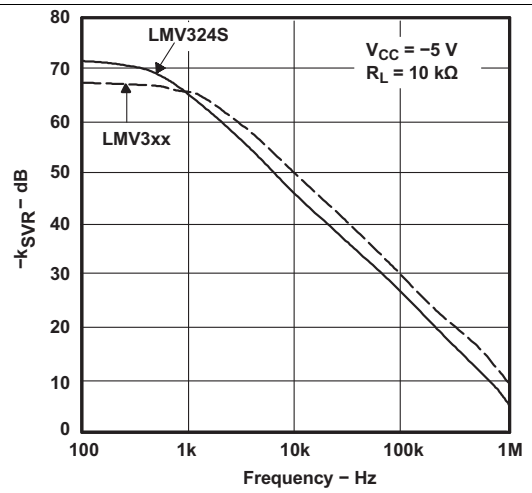


Figure 19. $-k_{SVR}$ vs Frequency

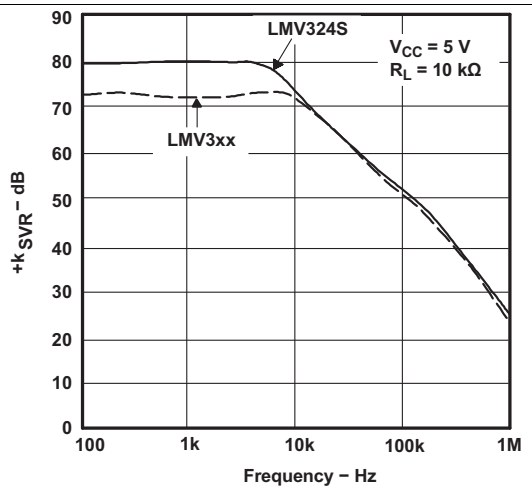


Figure 20. $+k_{SVR}$ vs Frequency

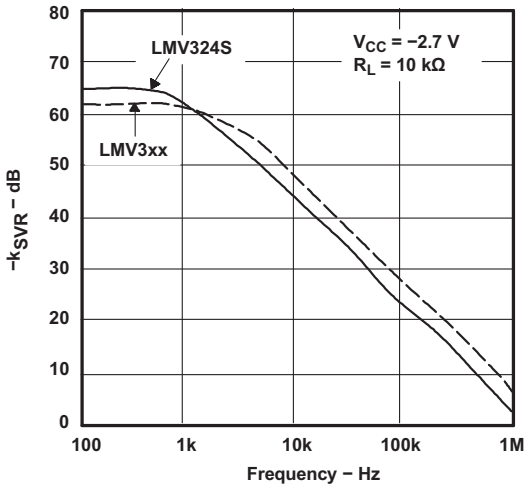


Figure 21. $-k_{SVR}$ vs Frequency

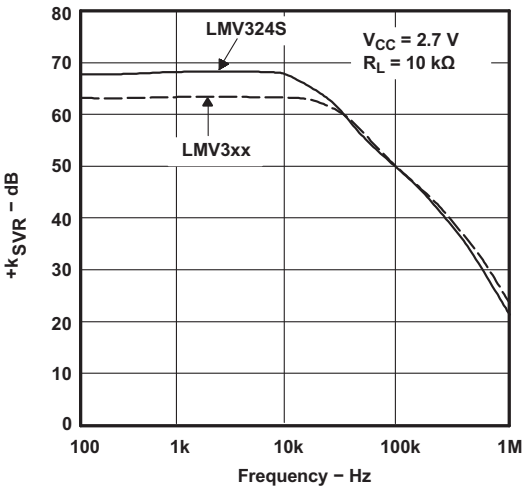


Figure 22. $+k_{SVR}$ vs Frequency

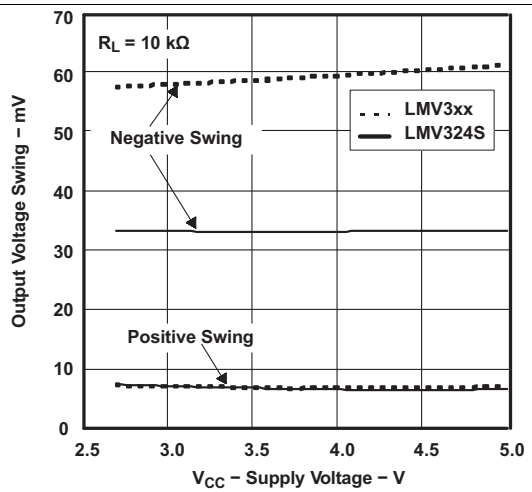


Figure 23. Output Voltage Swing From Rails vs Supply Voltage

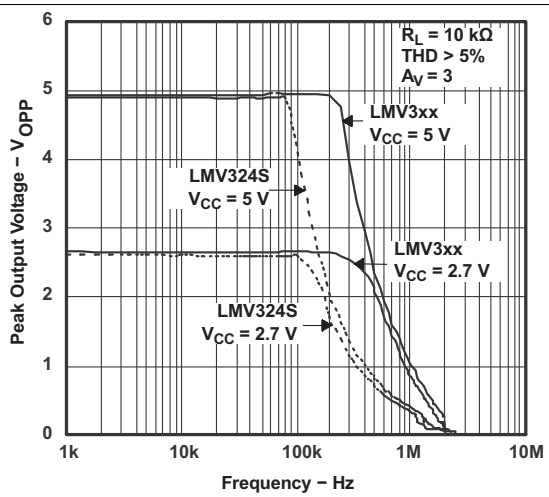


Figure 24. Output Voltage vs Frequency

Typical Characteristics (continued)

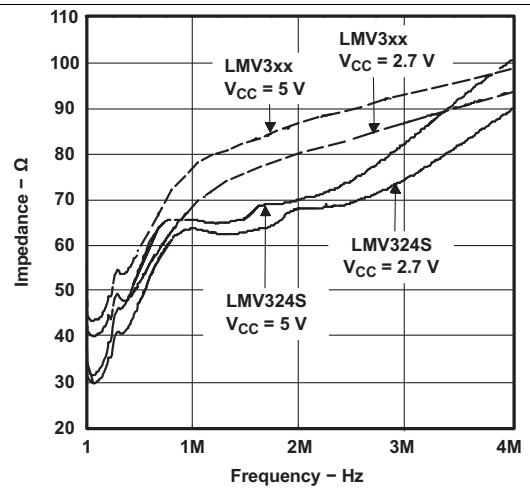


Figure 25. Open-Loop Output Impedence vs Frequency

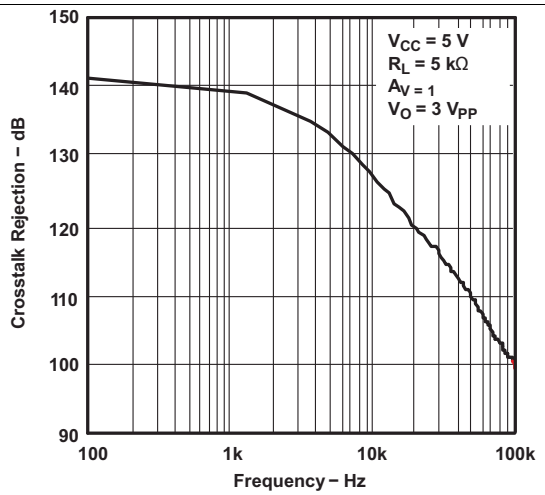


Figure 26. Cross-Talk Rejection vs Frequency

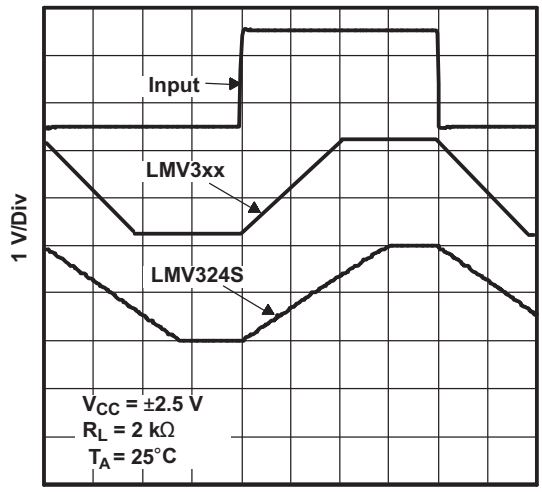


Figure 27. Noninverting Large-Signal Pulse Response

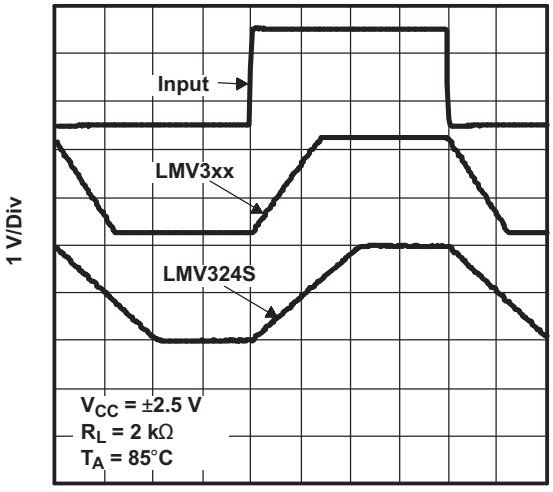


Figure 28. Noninverting Large-Signal Pulse Response

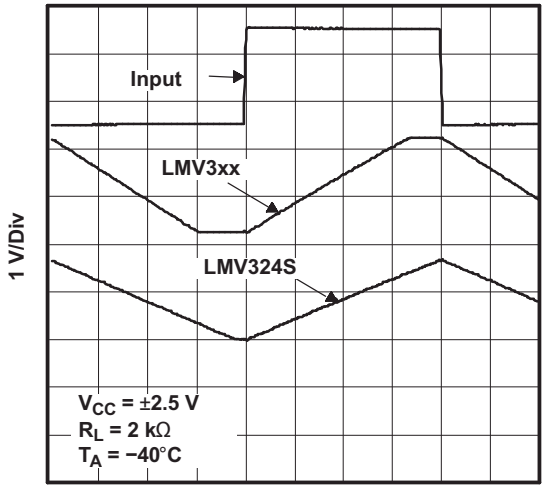


Figure 29. Noninverting Large-Signal Pulse Response

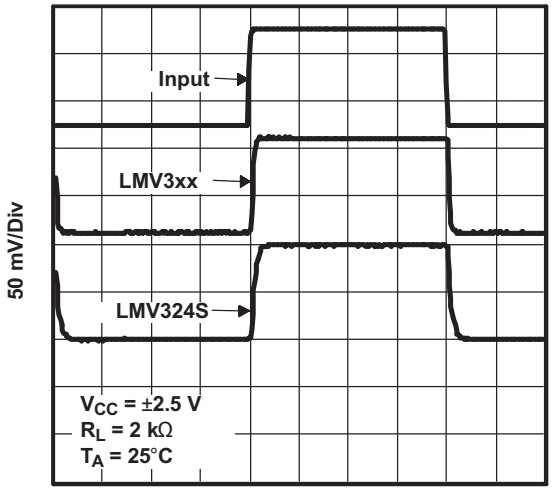


Figure 30. Noninverting Small-Signal Pulse Response

Typical Characteristics (continued)

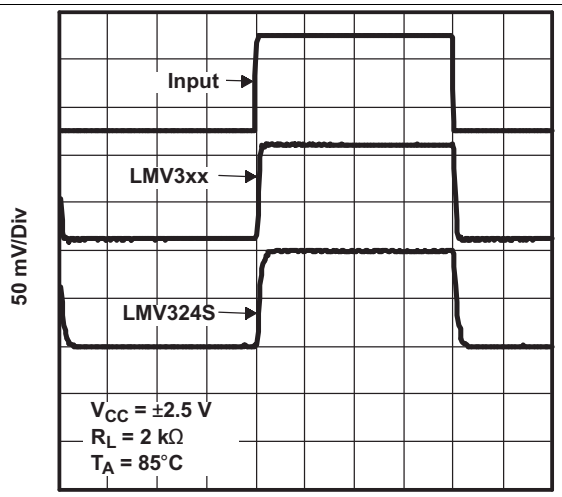


Figure 31. Noninverting Small-Signal Pulse Response

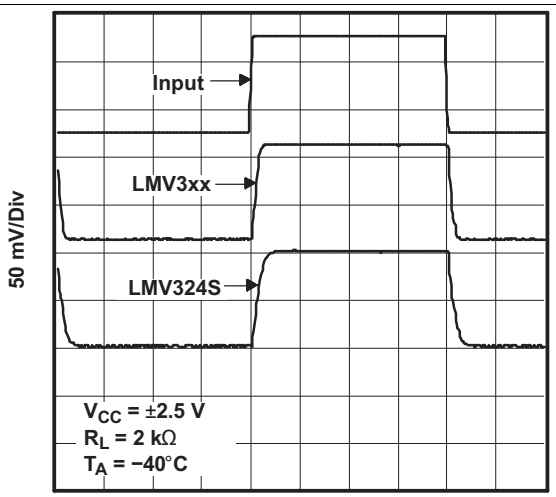


Figure 32. Noninverting Small-Signal Pulse Response

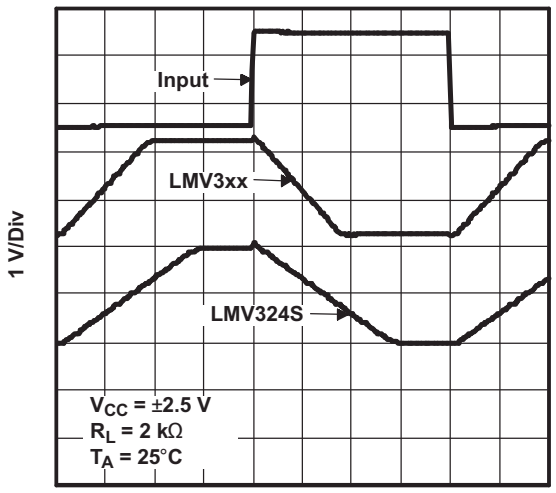


Figure 33. Inverting Large-Signal Pulse Response

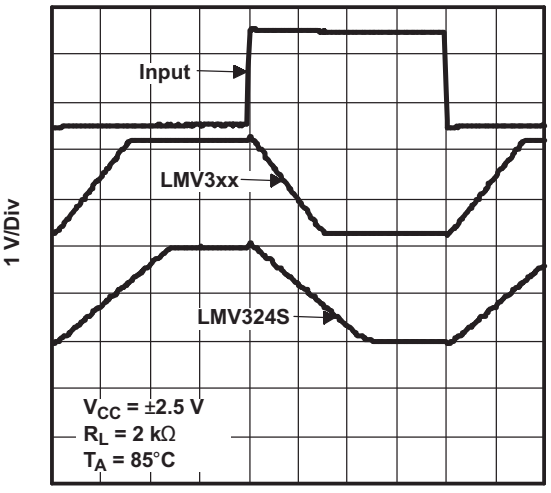


Figure 34. Inverting Large-Signal Pulse Response

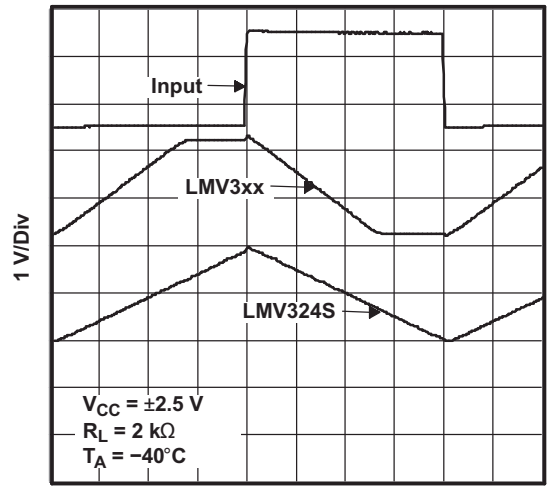


Figure 35. Inverting Large-Signal Pulse Response

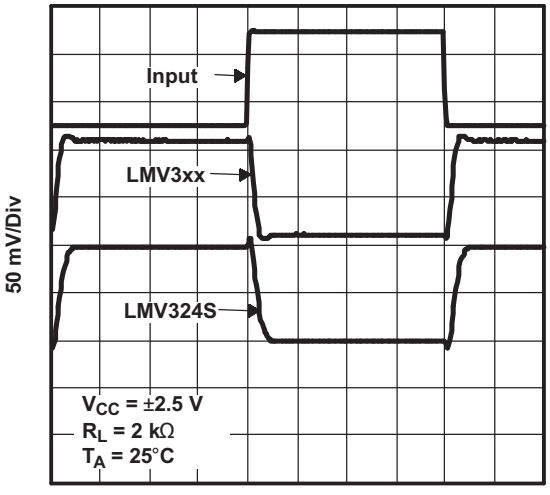


Figure 36. Inverting Small-Signal Pulse Response

Typical Characteristics (continued)

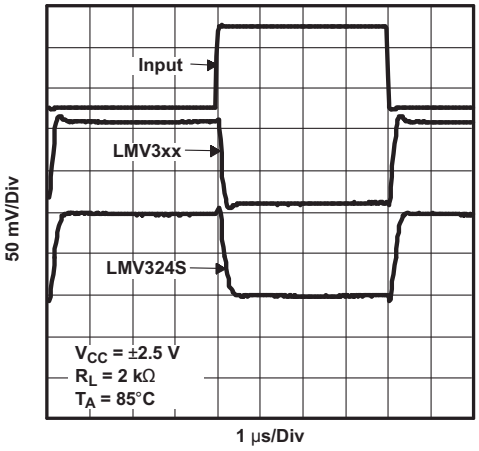


Figure 37. Inverting Small-Signal Pulse Response

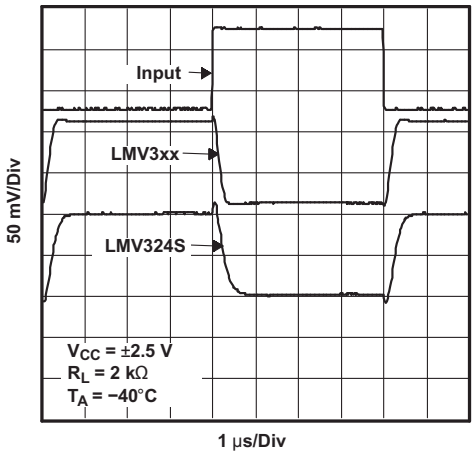


Figure 38. Inverting Small-Signal Pulse Response

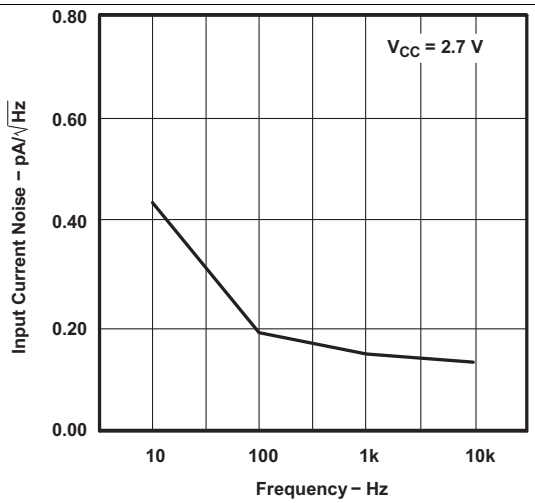


Figure 39. Input Current Noise vs Frequency

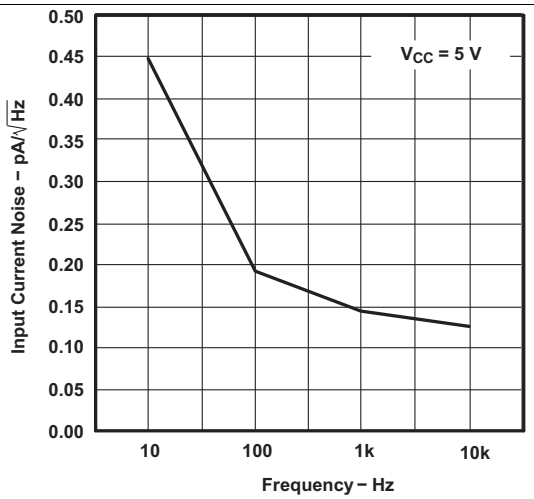


Figure 40. Input Current Noise vs Frequency

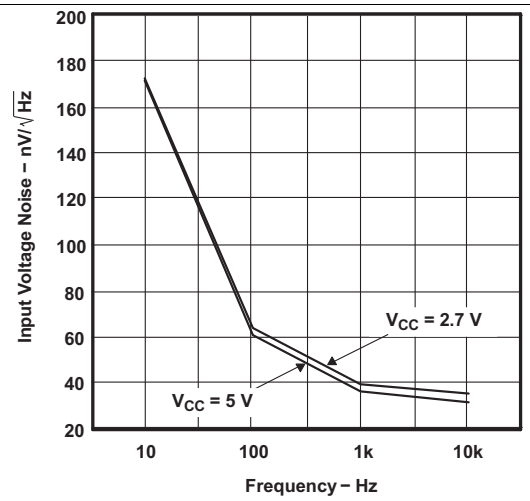


Figure 41. Input Voltage Noise vs Frequency

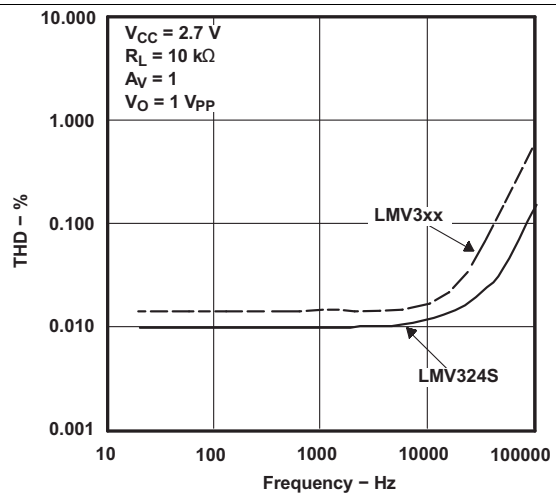


Figure 42. THD + N vs Frequency

Typical Characteristics (continued)

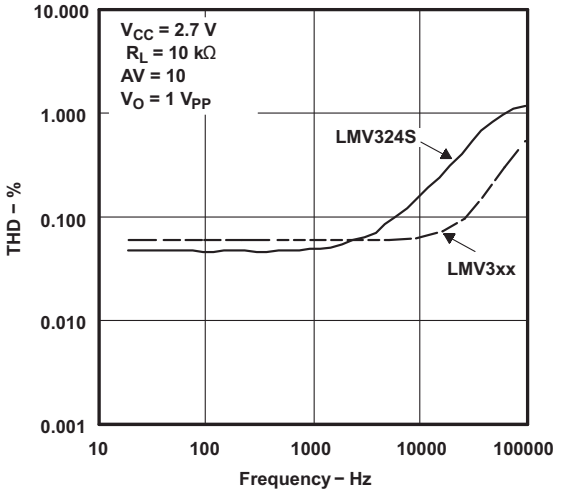


Figure 43. THD + N vs Frequency

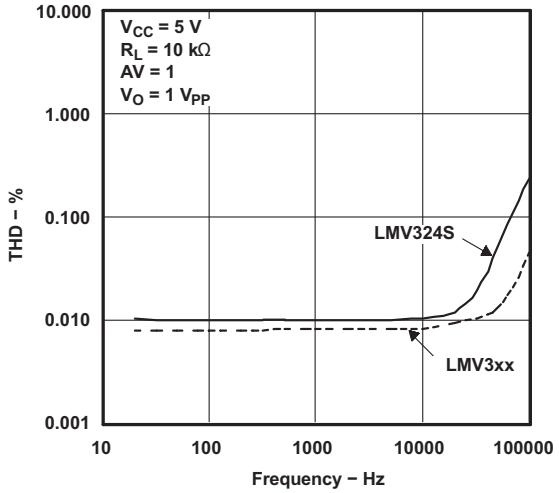


Figure 44. THD + N vs Frequency

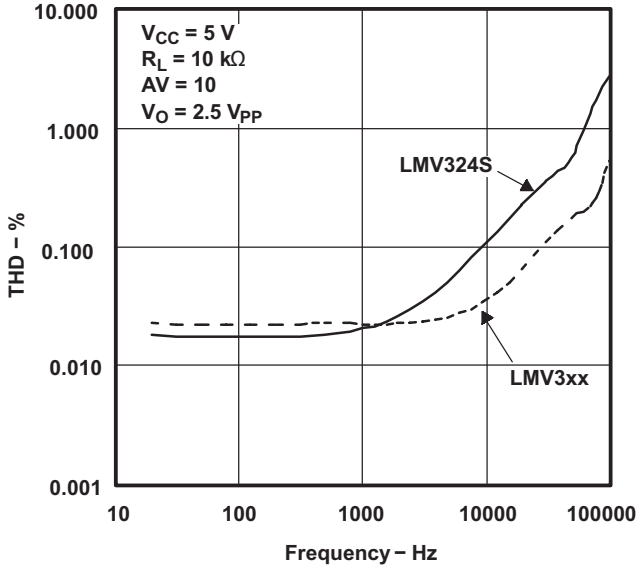


Figure 45. THD + N vs Frequency

8 Detailed Description

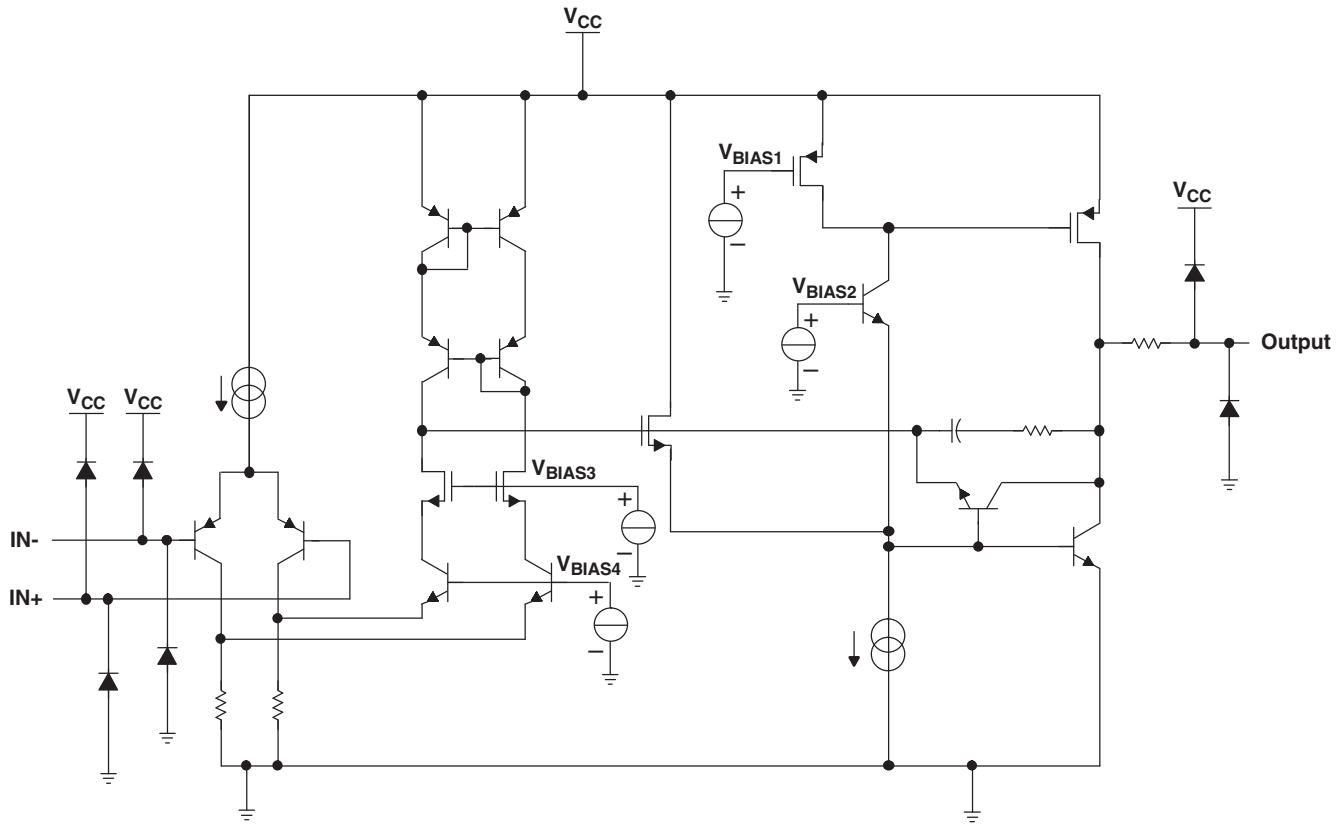
8.1 Overview

The LMV321, LMV358, LMV324, and LMV324S devices are single, dual, and quad low-voltage (2.7 V to 5.5 V) operational amplifiers with rail-to-rail output swing. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current when the amplifiers are not needed. Channels 1 and 2 together are put in shutdown, as are channels 3 and 4. While in shutdown, the outputs actively are pulled low.

The LMV321, LMV358, LMV324, and LMV324S devices are the most cost-effective solutions for applications where low-voltage operation, space saving, and low cost are needed. These amplifiers are designed specifically for low-voltage (2.7 V to 5 V) operation, with performance specifications meeting or exceeding the LM358 and LM324 devices that operate from 5 V to 30 V. Additional features of the LMV3xx devices are a common-mode input voltage range that includes ground, 1-MHz unity-gain bandwidth, and 1-V/μs slew rate.

The LMV321 device is available in the ultra-small package, which is approximately one-half the size of the DBV (SOT-23) package. This package saves space on printed circuit boards and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The LMV321, LMV358, LMV324, LMV324S devices are fully specified and ensured for operation from 2.7 V to 5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are shown in the *Typical Characteristics* graphs.

8.3.2 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The LMV321, LMV358, LMV324, LMV324S devices have a 1-MHz unity-gain bandwidth.

8.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The LMV321, LMV358, LMV324, LMV324S devices have a 1-V/μs slew rate.

8.4 Device Functional Modes

The LMV321, LMV358, LMV324, LMV324S devices are powered on when the supply is connected. The LMV324S device, which is a variation of the standard LMV324 device, includes a power-saving shutdown feature that reduces supply current to a maximum of 5 μA per channel when the amplifiers are not needed. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

Some applications require differential signals. Figure 46 shows a simple circuit to convert a single-ended input of 0.5 to 2 V into differential output of ±1.5 V on a single 2.7-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-}. Both V_{OUT+} and V_{OUT-} range from 0.5 to 2 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and V_{OUT-}. The LMV358 was used to build this circuit.

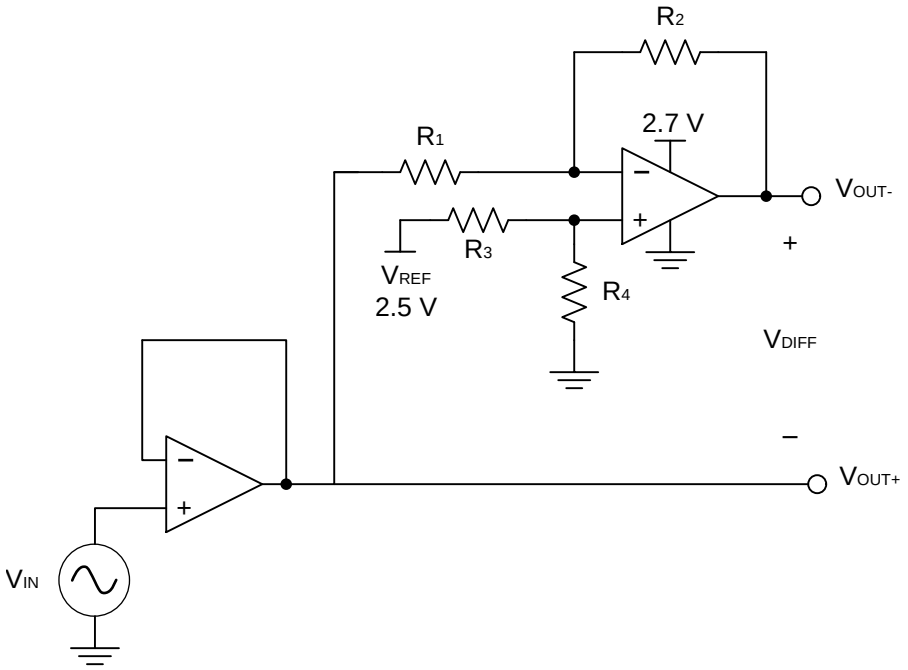


Figure 46. Schematic for Single-Ended Input to Differential Output Conversion

Typical Application (continued)

9.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 2.7 V
- Reference voltage: 2.5 V
- Input: 0.5 to 2 V
- Output differential: ±1.5 V

9.1.2 Detailed Design Procedure

The circuit in Figure 46 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} (see Equation 1). V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{OUT-} = V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(1 + \frac{R_2}{R_1}\right) - V_{IN} \times \frac{R_2}{R_1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

9.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Because LMV358 has a bandwidth of 1 MHz, this circuit will only be able to process signals with frequencies of less than 1 MHz.

9.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. If the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

Typical Application (continued)

9.1.3 Application Curves

The measured transfer functions in Figure 47, Figure 48, and Figure 49 were generated by sweeping the input voltage from 0 V to 2.5 V. However, this design should only be used between 0.5 V and 2 V for optimum linearity.

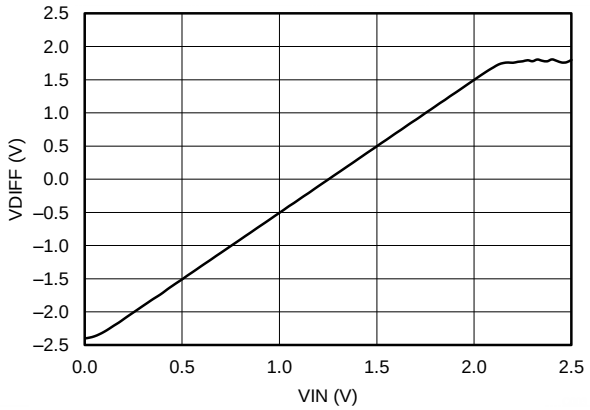


Figure 47. Differential Output Voltage vs Input Voltage

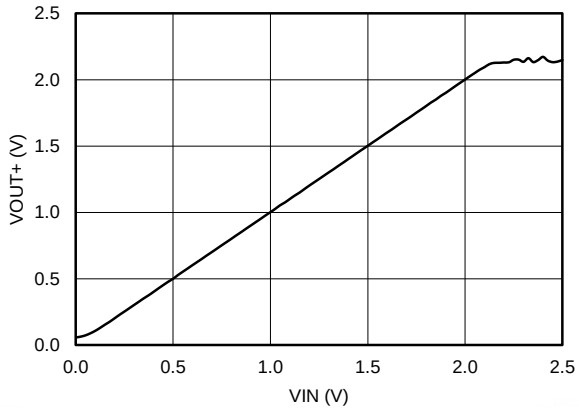


Figure 48. Positive Output Voltage Node vs Input Voltage

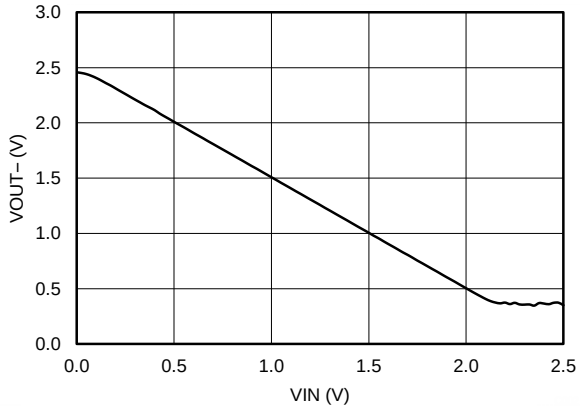


Figure 49. Positive Output Voltage Node vs Input Voltage

10 Power Supply Recommendations

The LMV321, LMV358, LMV324, LMV324S devices are specified for operation from 2.7 to 5 V; many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 5.5 V can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

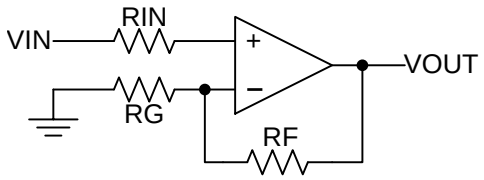


Figure 50. Operational Amplifier Schematic for Noninverting Configuration

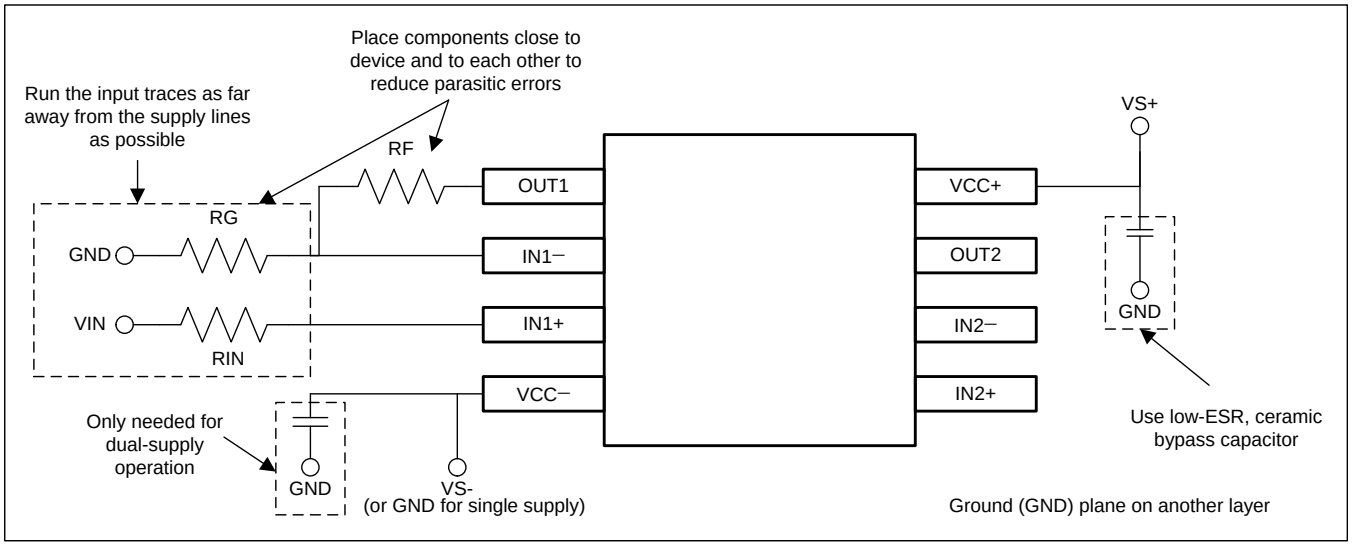


Figure 51. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMV321	Click here	Click here	Click here	Click here	Click here
LMV358	Click here	Click here	Click here	Click here	Click here
LMV324	Click here	Click here	Click here	Click here	Click here
LMV324S	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F, RC1K)	Samples
LMV321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F, RC1K)	Samples
LMV321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F, RC1K)	Samples
LMV321IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F, RC1K)	Samples
LMV321IDBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RC1F, RC1K)	Samples
LMV321IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3F, R3K, R3O, R3R, R3Z)	Samples
LMV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R3F, R3K, R3O, R3R, R3Z)	Samples
LMV321IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(R3C, R3F, R3R)	Samples
LMV324ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324I	Samples
LMV324IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples
LMV324IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples
LMV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324I	Samples
LMV324QD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV324QDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	LMV324Q	Samples
LMV324QPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV324QPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV324QPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV324Q	Samples
LMV358ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RA5R	Samples
LMV358IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RA5R	Samples
LMV358IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R5B, R5Q, R5R)	Samples
LMV358IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(R5B, R5Q, R5R)	Samples
LMV358IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358IPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV358IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358I	Samples
LMV358QD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAHR	Samples
LMV358QDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	RAHR	Samples
LMV358QDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RHO, RHR)	Samples
LMV358QDGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	(RHO, RHR)	Samples
LMV358QDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples
LMV358QPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	MV358Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

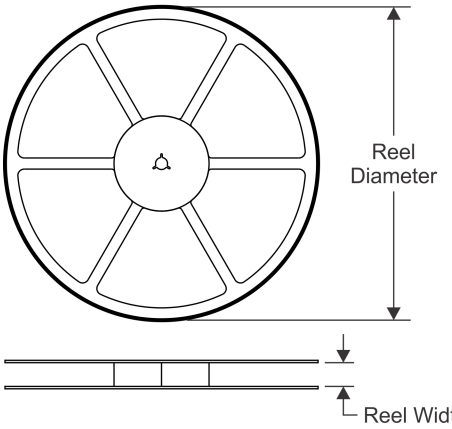
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

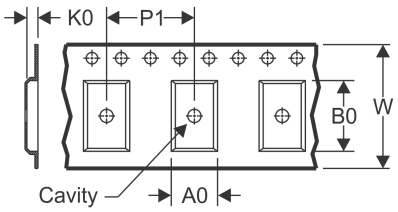
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

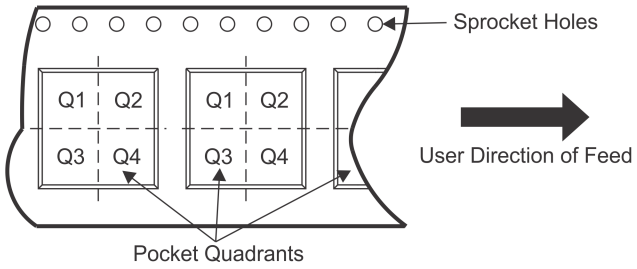


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

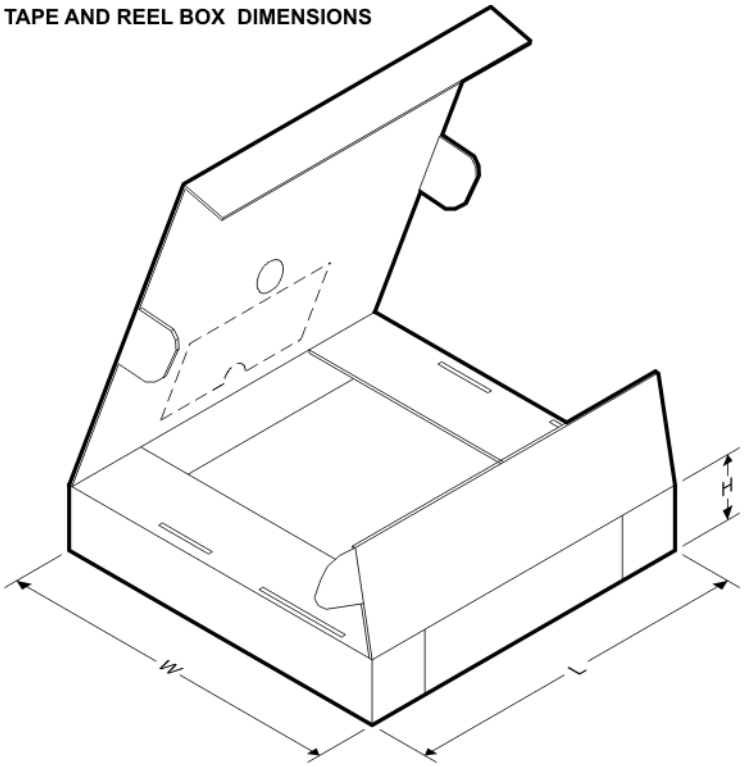


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV321IDCKR	SC70	DCK	5	3000	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	180.0	9.2	2.3	2.55	1.2	4.0	8.0	Q3
LMV321IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LMV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324IPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV324QDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV324QPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LMV358IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IDR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358IPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LMV358QDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LMV358QDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV358QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV358QPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



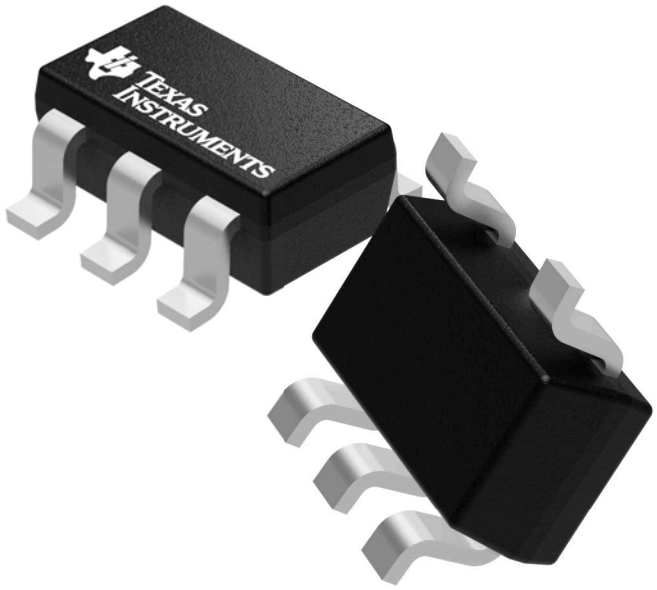
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LMV321IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LMV321IDCKR	SC70	DCK	5	3000	205.0	200.0	33.0
LMV321IDCKT	SC70	DCK	5	250	205.0	200.0	33.0
LMV321IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
LMV324IDR	SOIC	D	14	2500	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV324IDR	SOIC	D	14	2500	364.0	364.0	27.0
LMV324IDR	SOIC	D	14	2500	333.2	345.9	28.6
LMV324IDRG4	SOIC	D	14	2500	333.2	345.9	28.6
LMV324IPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324IPWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LMV324IPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV324QDR	SOIC	D	14	2500	367.0	367.0	38.0
LMV324QPWR	TSSOP	PW	14	2000	367.0	367.0	35.0
LMV358IDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358IDR	SOIC	D	8	2500	367.0	367.0	35.0
LMV358IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IDR	SOIC	D	8	2500	364.0	364.0	27.0
LMV358IDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LMV358IPWR	TSSOP	PW	8	2000	364.0	364.0	27.0
LMV358IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358IPWRG4	TSSOP	PW	8	2000	367.0	367.0	35.0
LMV358QDDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LMV358QDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LMV358QDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV358QPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

DBV 5 SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



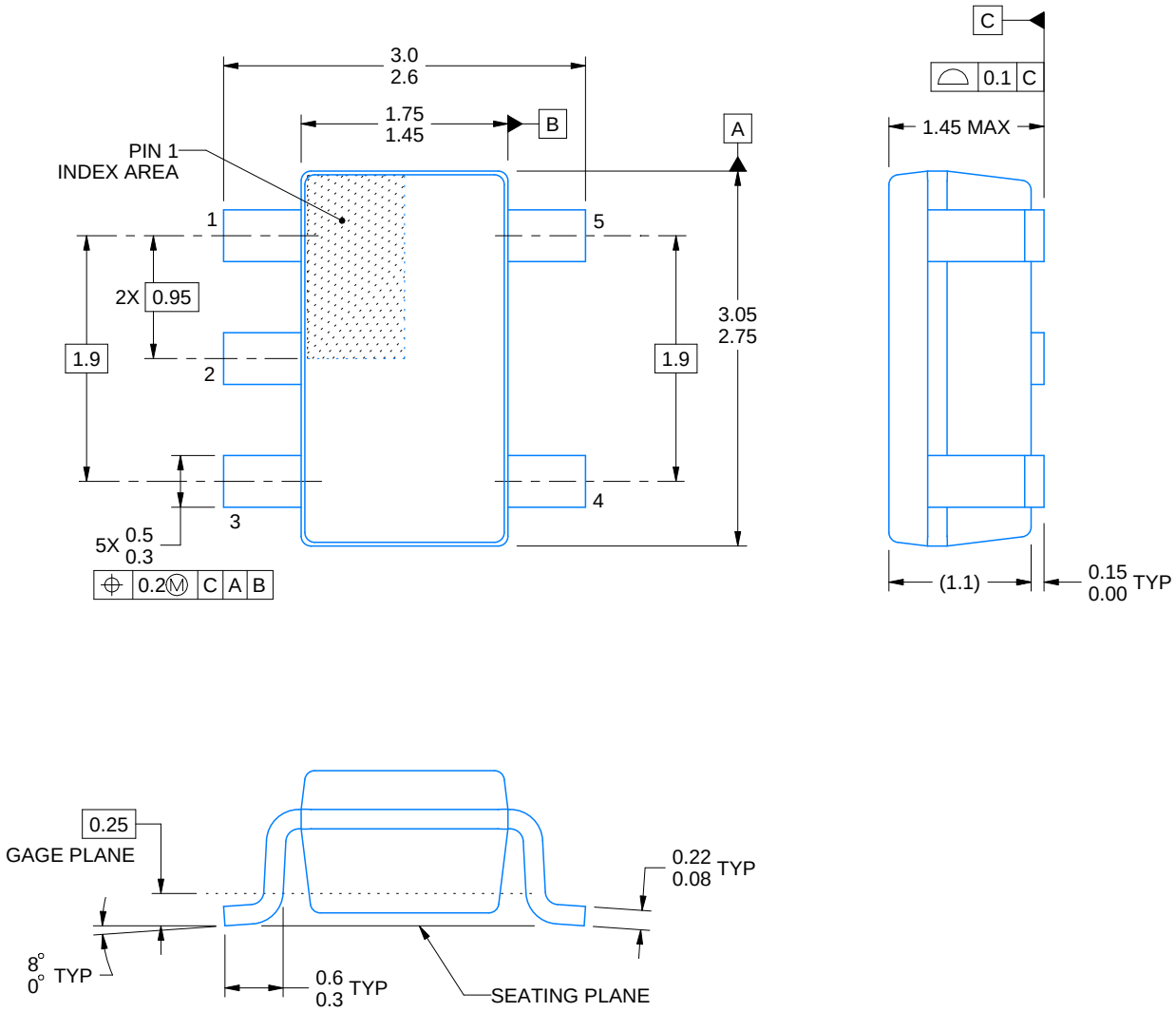
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

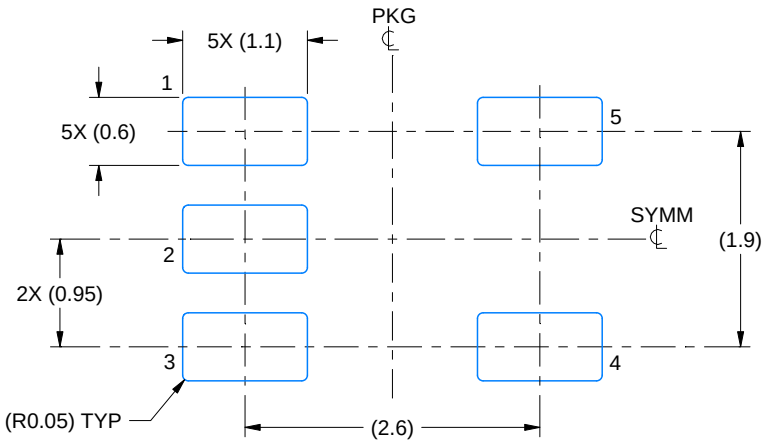
SMALL OUTLINE TRANSISTOR



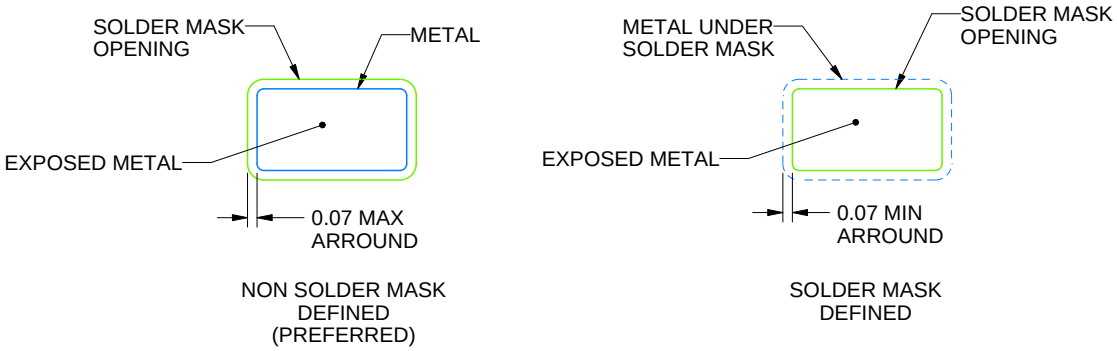
4214839/D 11/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

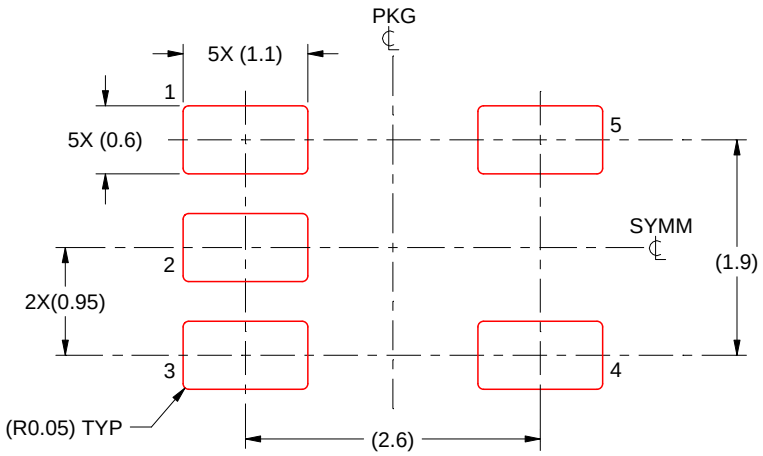


SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



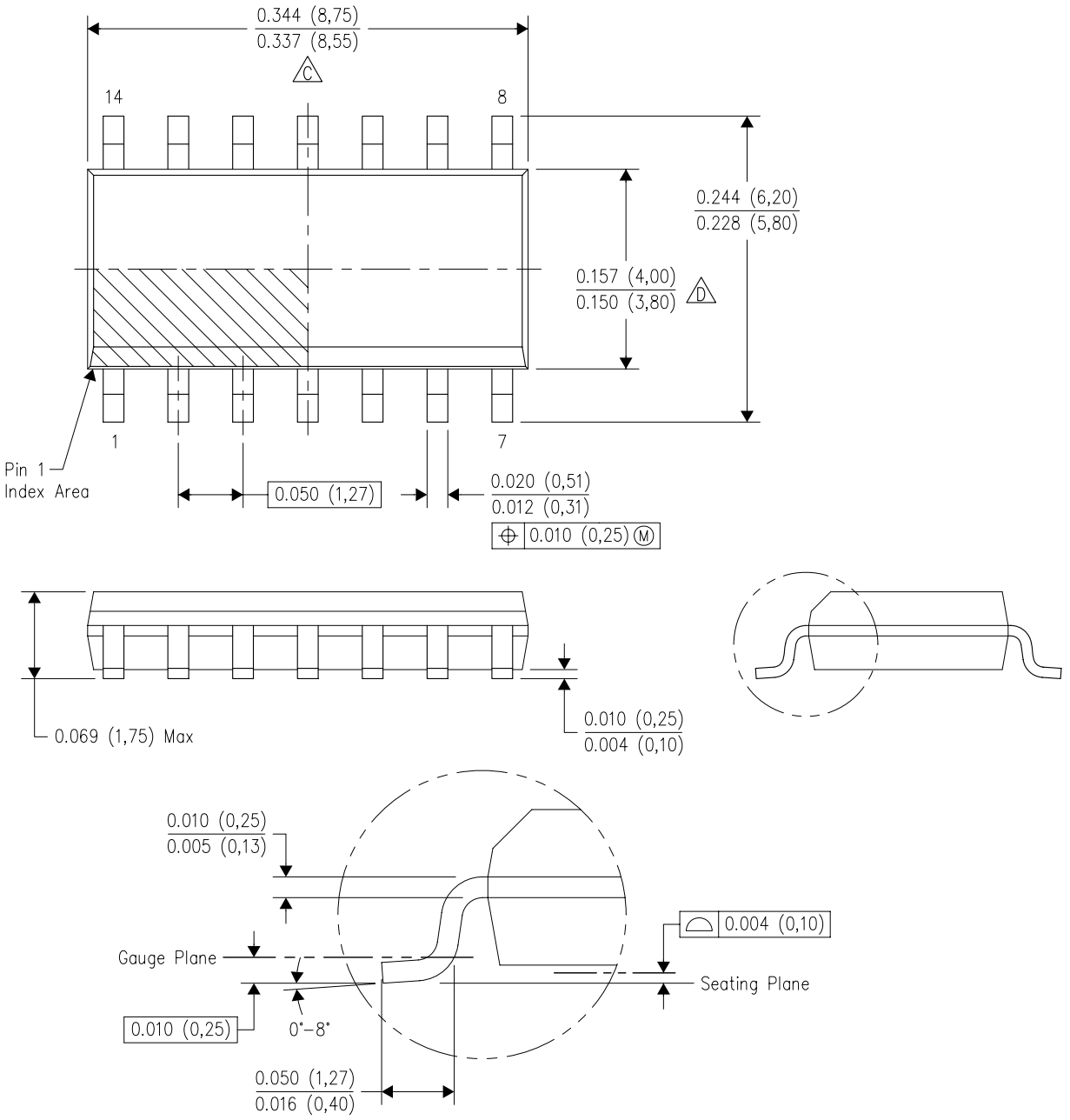
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

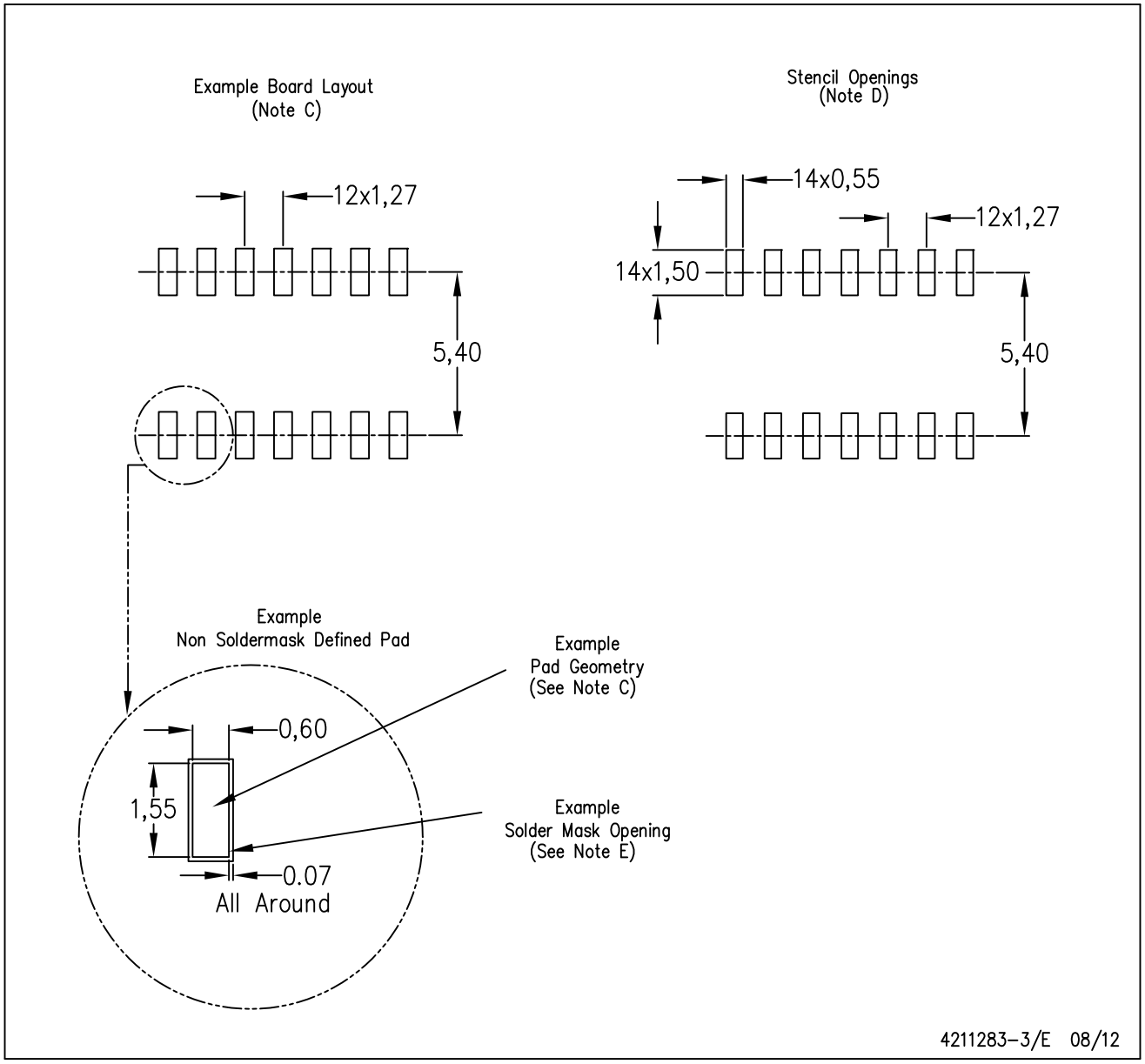
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

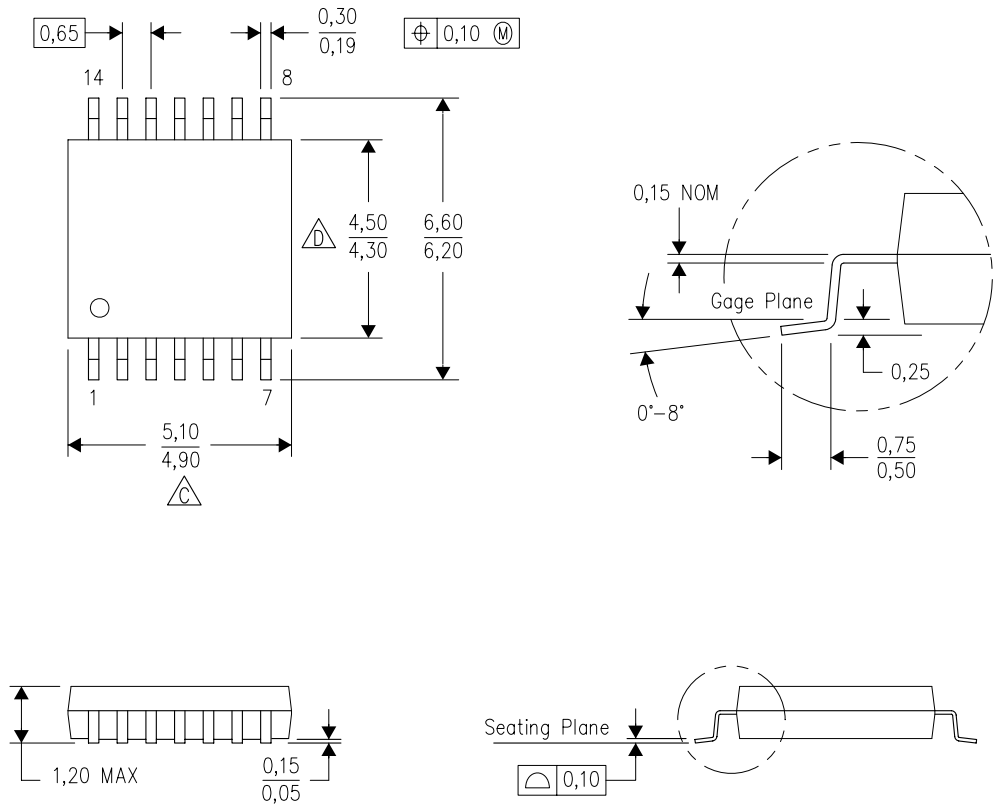
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

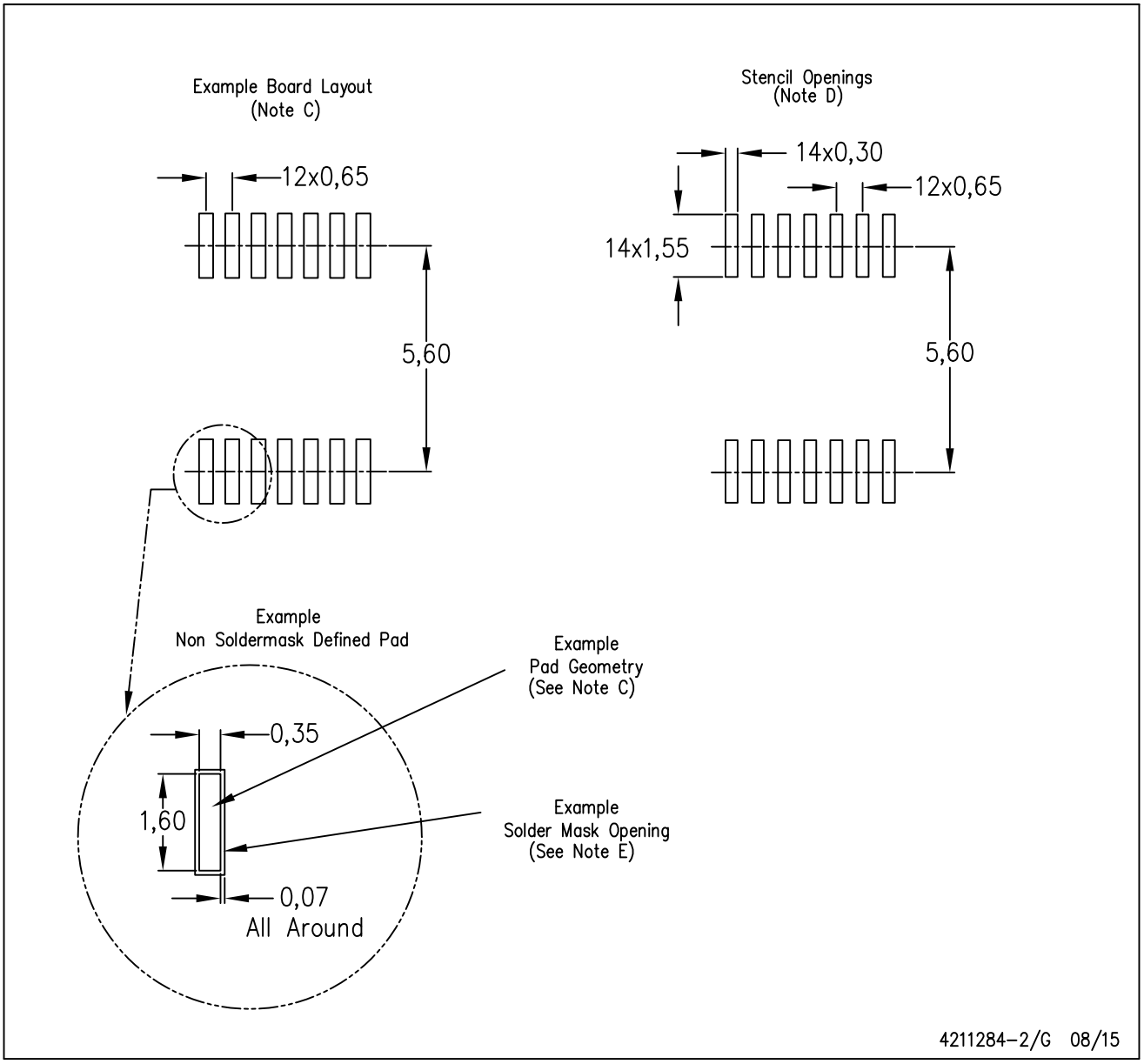
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

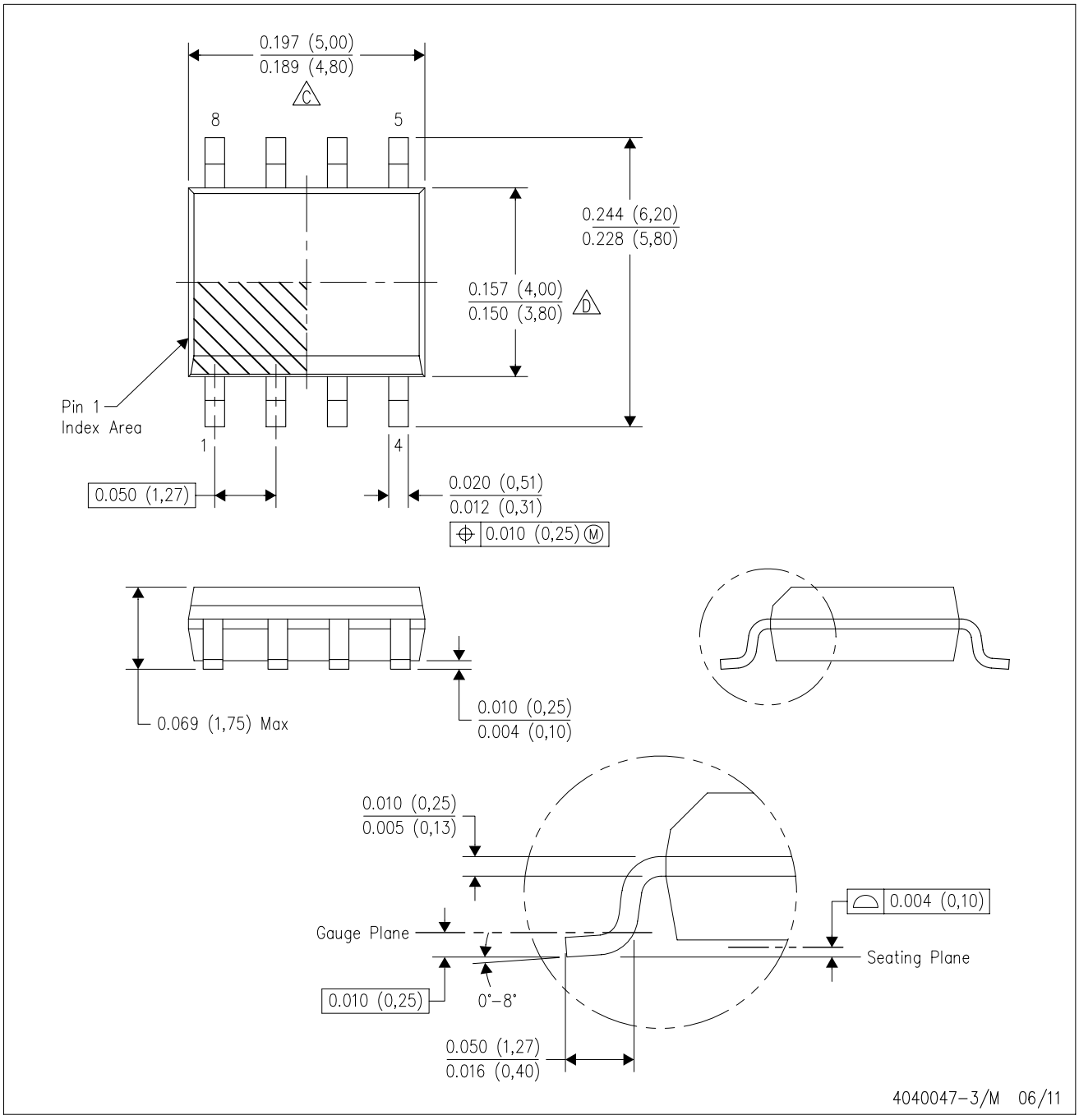
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

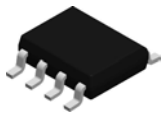


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

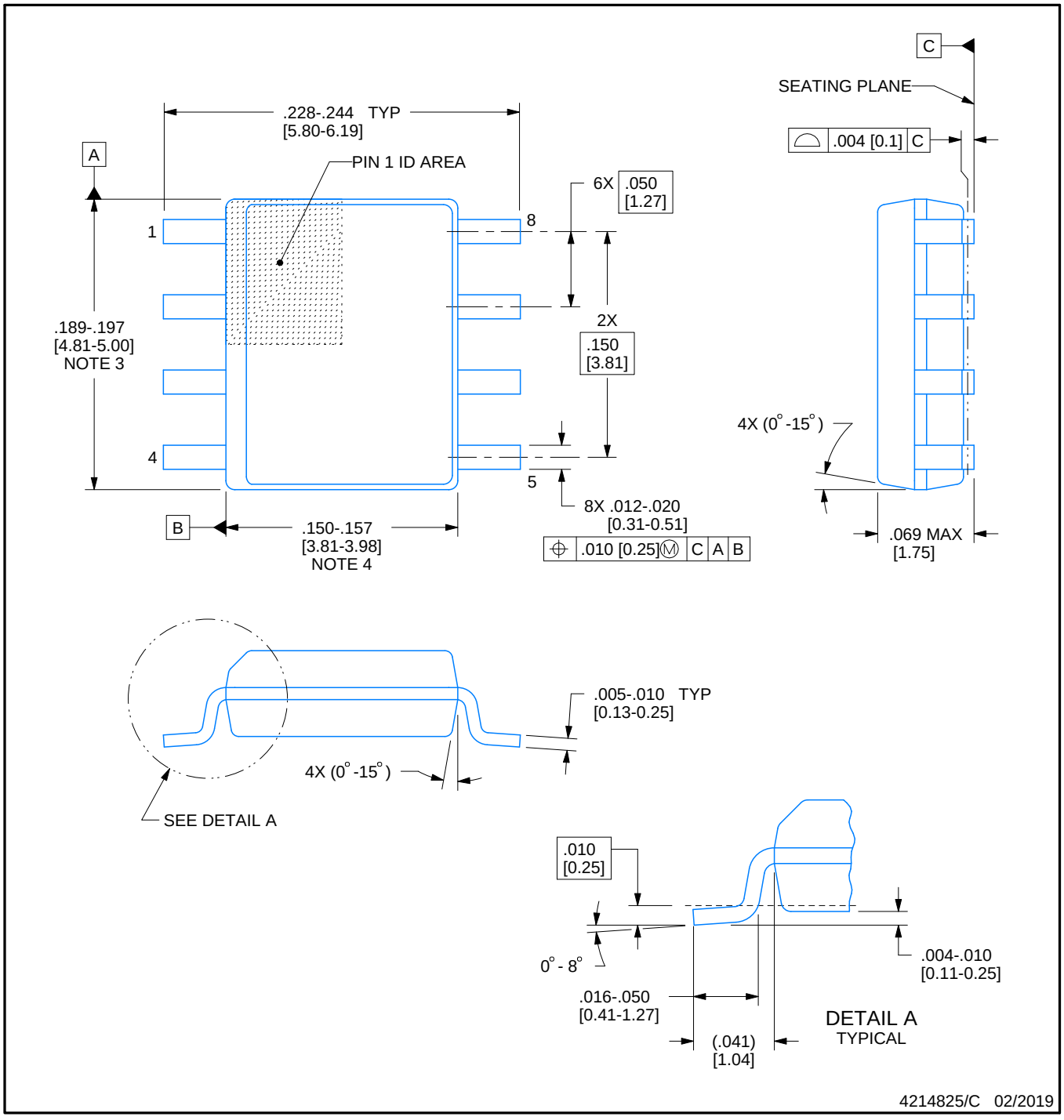


PACKAGE OUTLINE

D0008A

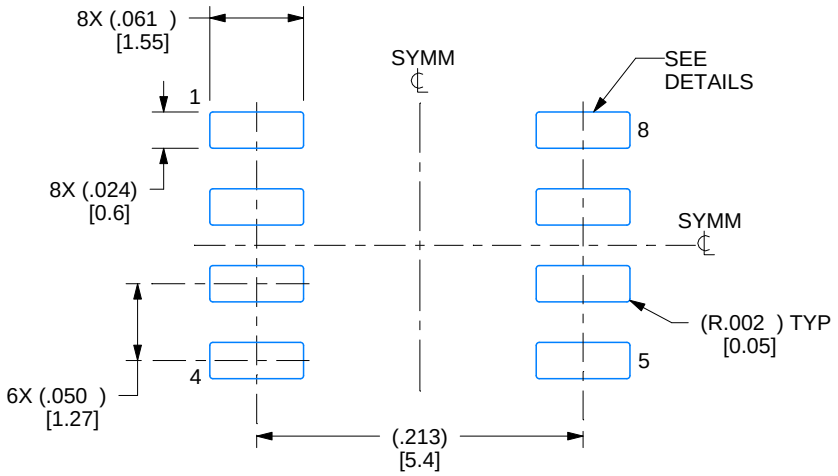
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

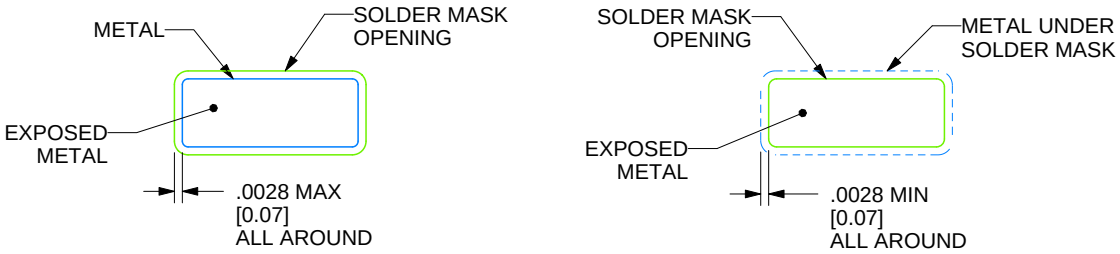


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

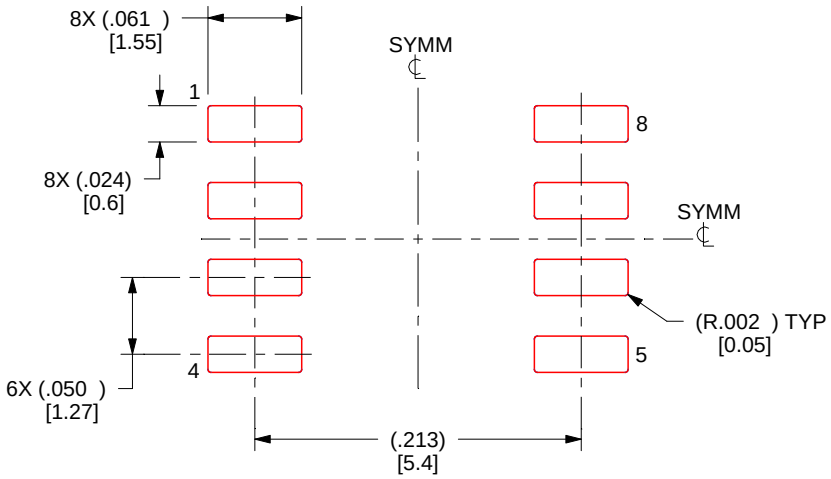
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



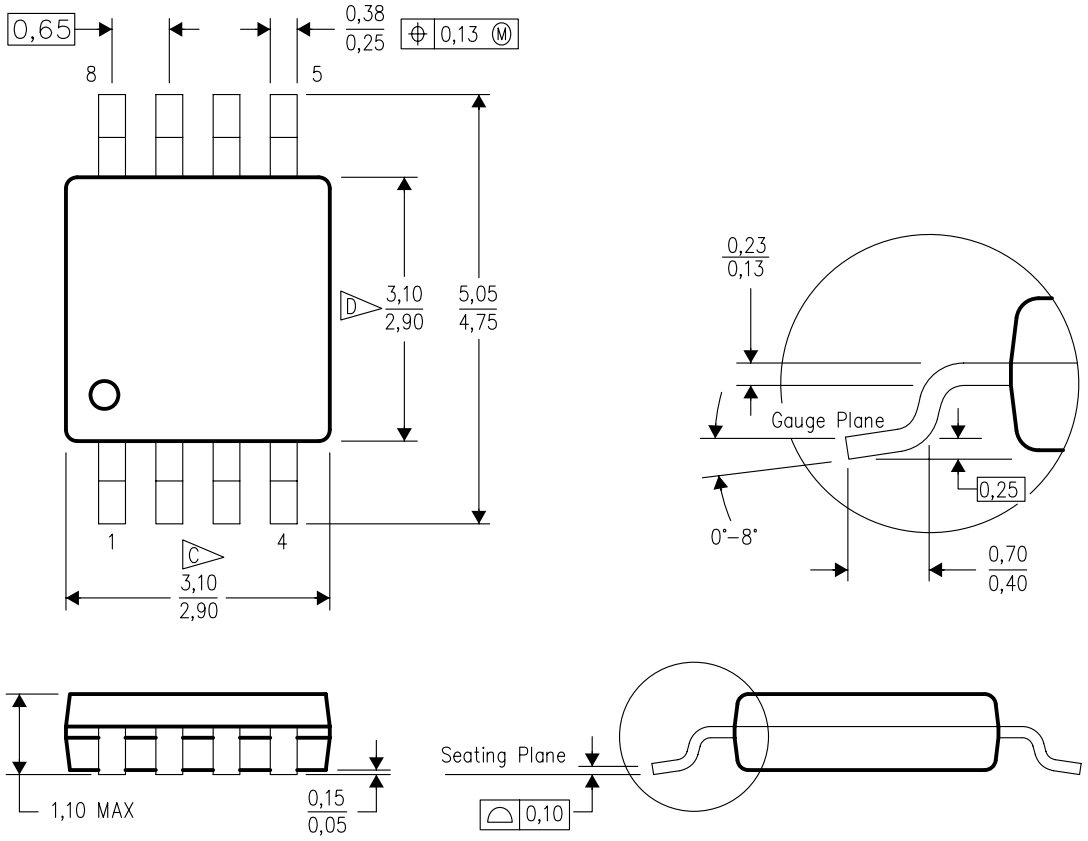
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

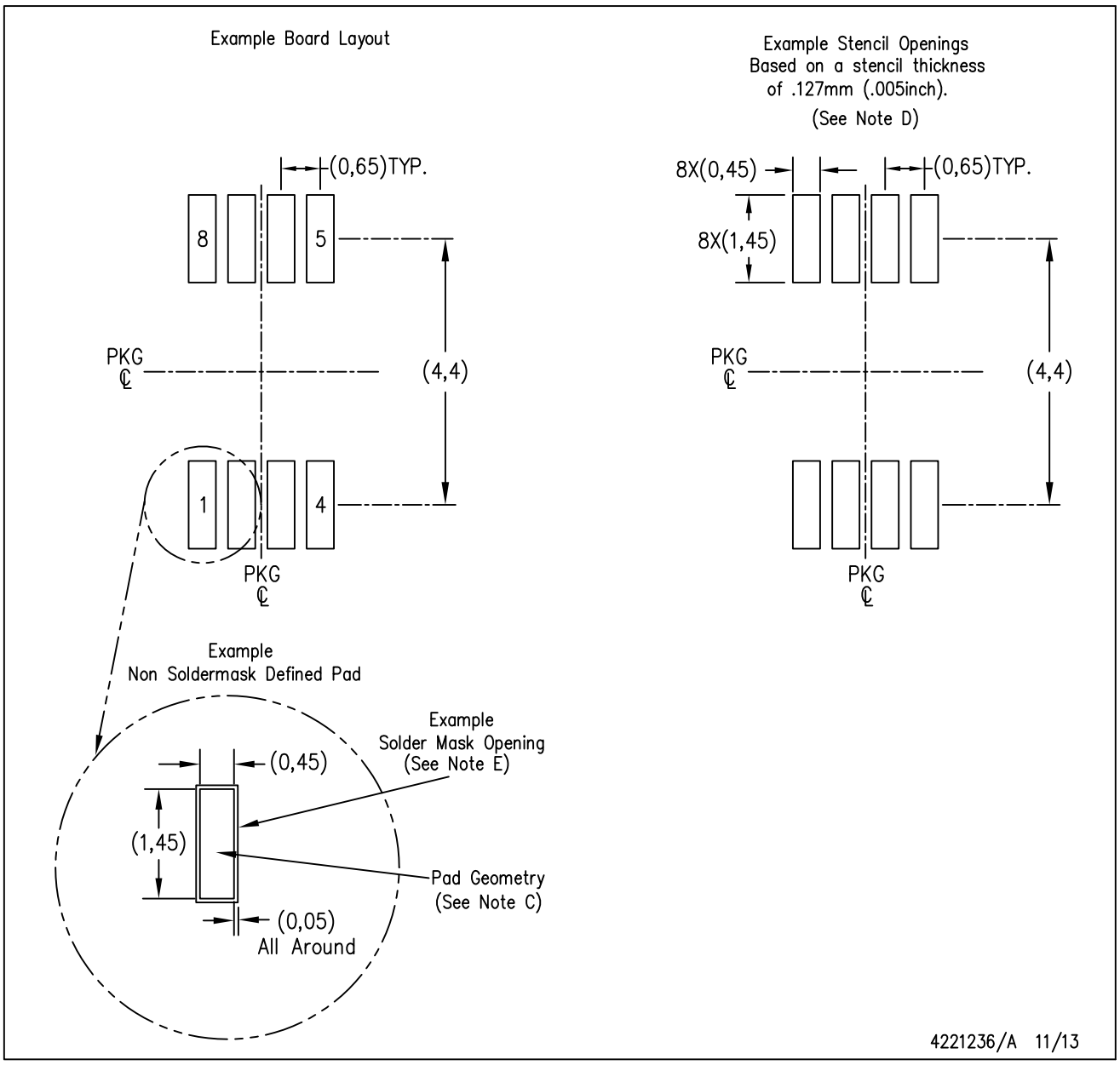
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



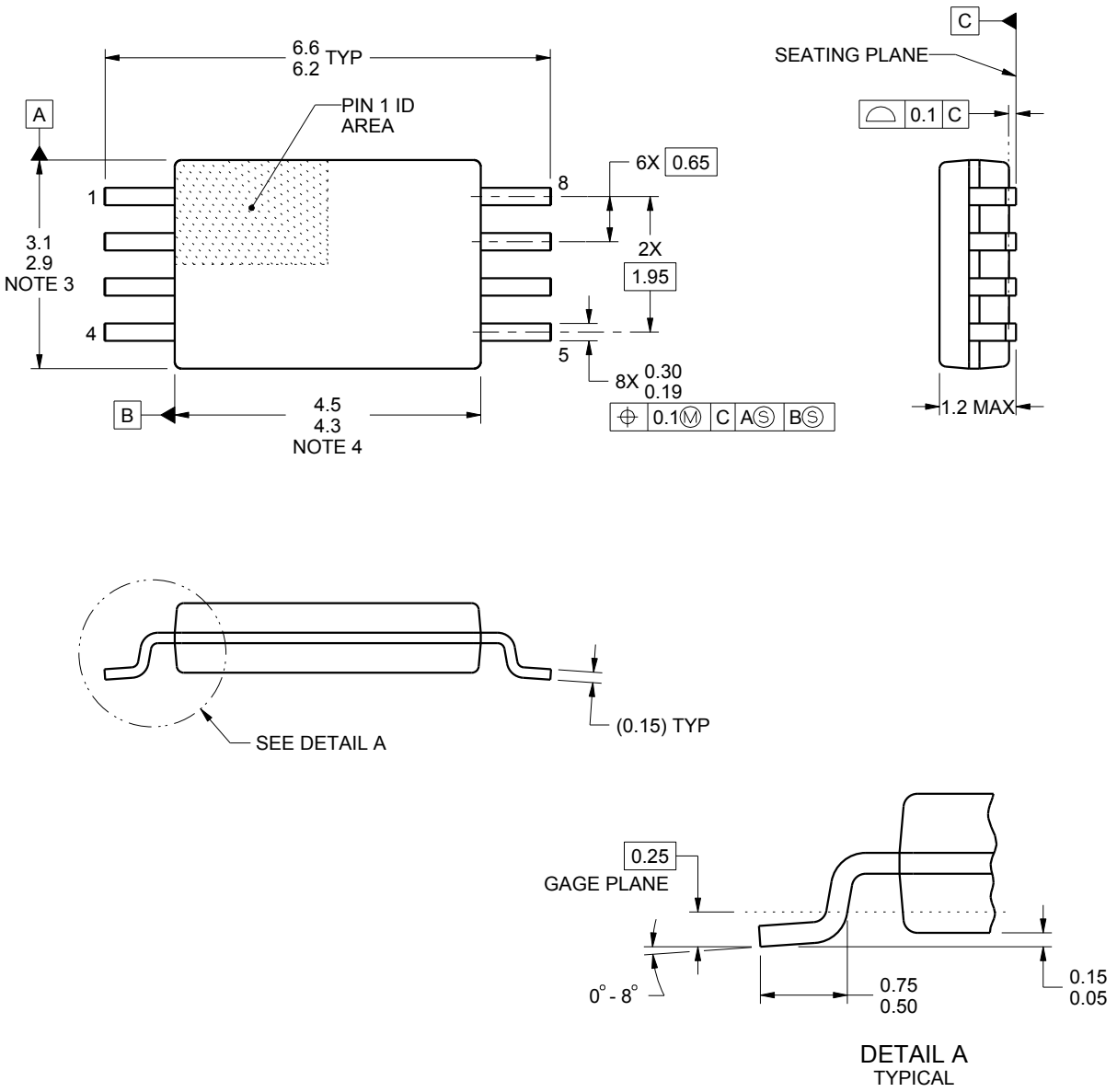
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0008A

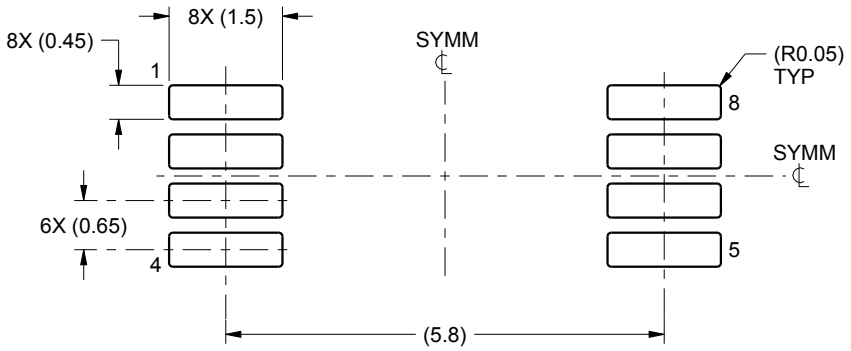
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

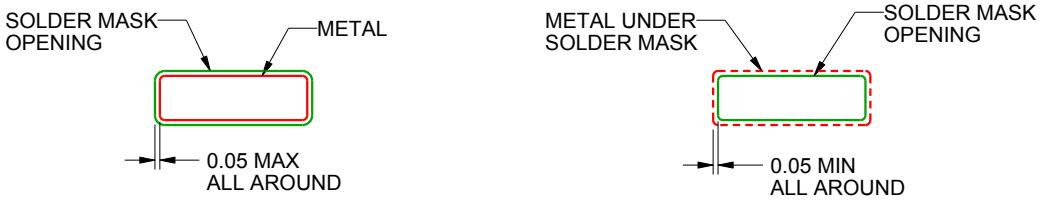


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

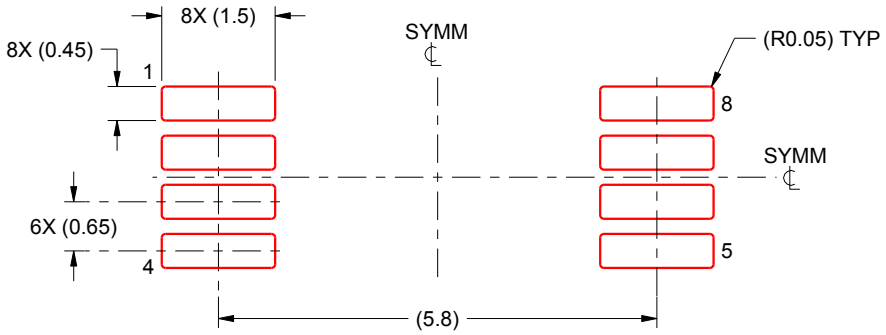


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



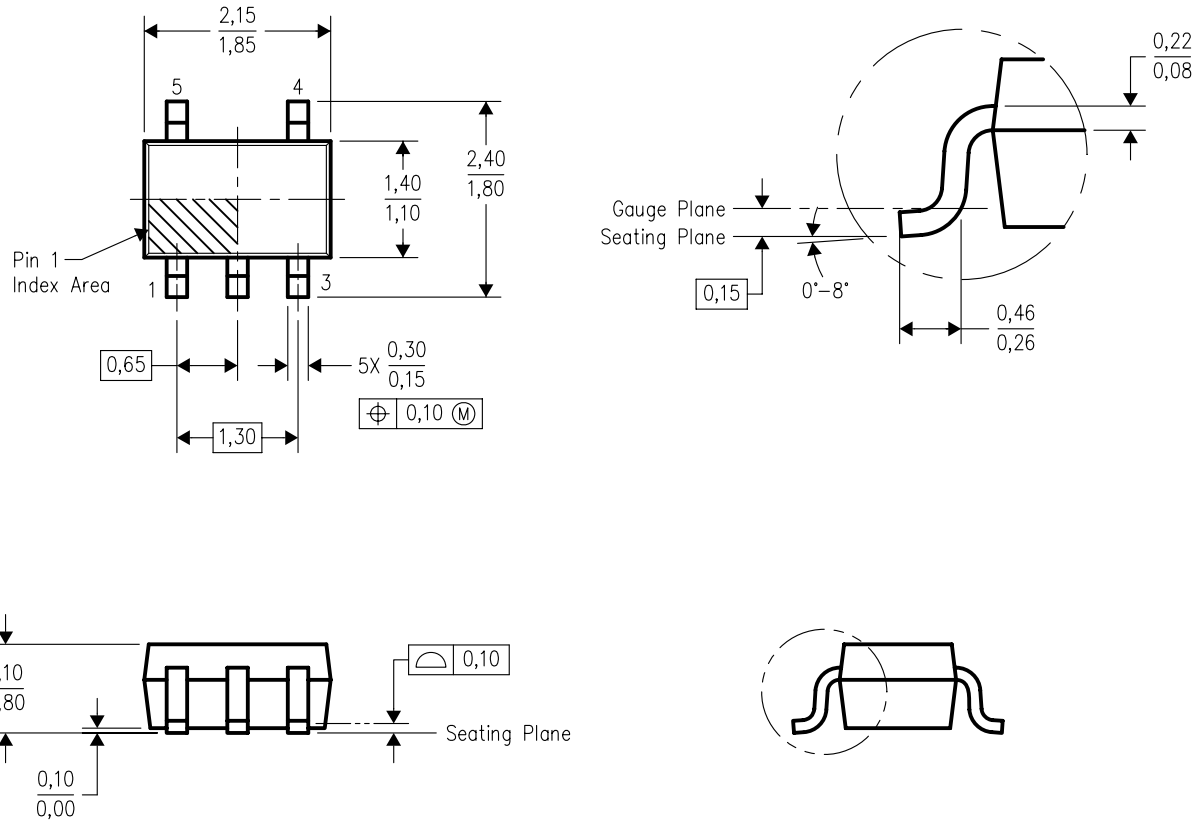
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

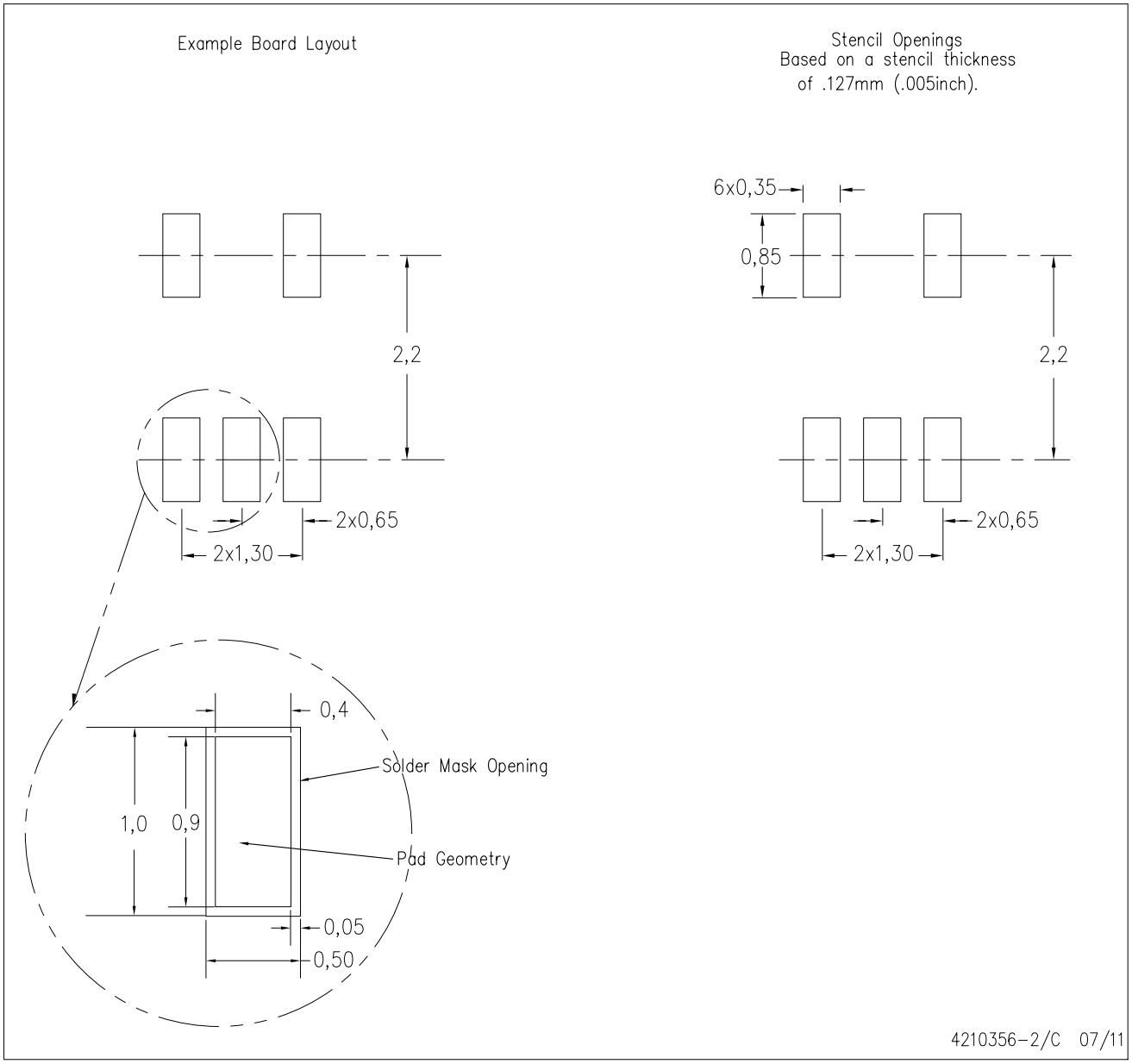
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

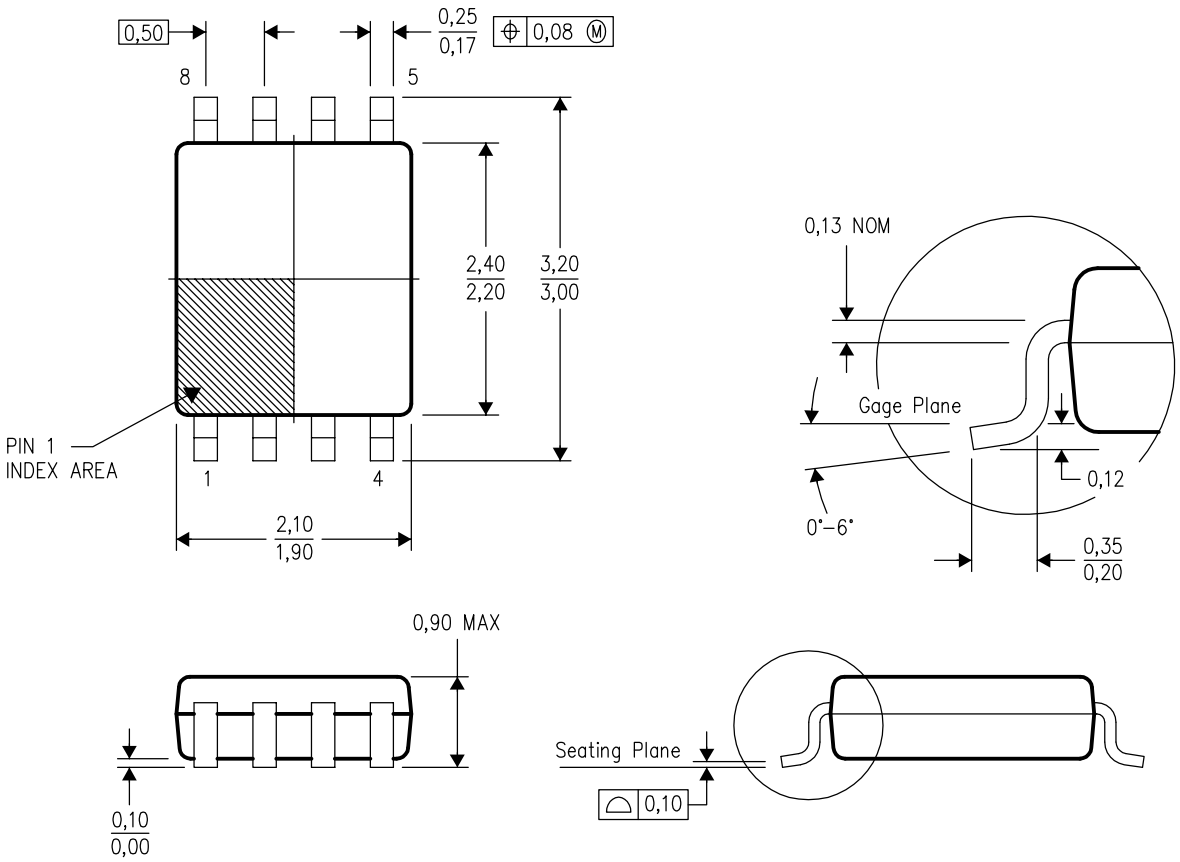
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

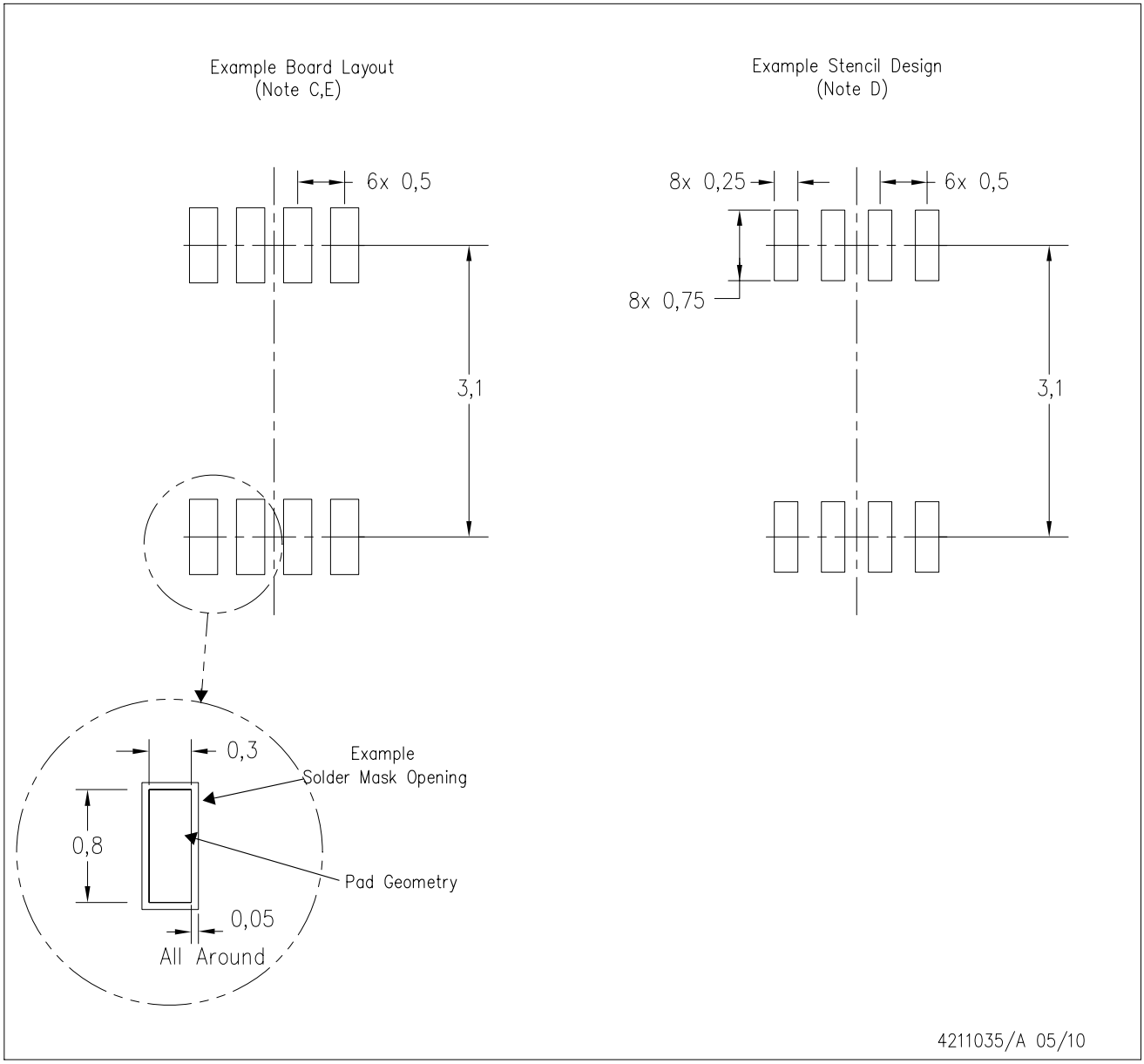
DDU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4205140/A 05/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation CA.

DDU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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