Precision, Very Low Noise, Low Input Bias Current, Wide Bandwidth JFET Operational Amplifiers

AD8512

FEATURES

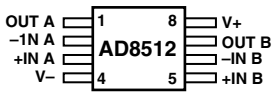
Fast Settling Time: 500 ns to 0.1%
Low Offset Voltage: 400 μV Max
Low TcVos: 1 μV/°C Typ
Low Input Bias Current: 25 pA Typ
Dual-Supply Operation: ±5 V to ±15 V
Low Noise: 8 nV/√Hz
Low Distortion: 0.0005%
No Phase Reversal
Unity Gain Stable

APPLICATIONS

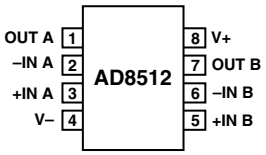
Instrumentation
Multi-Pole Filters
Precision Current Measurement
Photodiode Amplifiers
Sensors
Audio

PIN CONFIGURATIONS

8-Lead MSOP
(RM Suffix)



8-Lead SOIC
(R Suffix)



GENERAL DESCRIPTION

The AD8512 is a dual precision JFET amplifier featuring low offset voltage, low input bias current, low input voltage noise, and low input current noise.

The combination of low offsets, low noise, and very low input bias currents makes this amplifier especially suitable for high impedance sensor amplification and precise current measurements using shunts. The combination of dc precision, low noise, and fast settling time results in superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the AD8512 maintains its fast settling performance even with substantial capacitive loads.

Fast slew rate and great stability with capacitive loads make the AD8512 a perfect fit for high-performance filters.

Low input bias currents, low offset, and low noise result in wide dynamic range in photodiode amplifier circuits.

Low noise and distortion, high output current, and excellent speed make the AD8512 a great choice for stereo audio applications.

Unlike many older JFET amplifiers, the AD8512 does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

The AD8512 is available in 8-lead narrow SOIC and 8-lead mini-SOIC packages. Mini-SOIC packaged parts are only available in tape and reel.

The AD8512 is specified over the extended industrial (–40°C to +125°C) temperature range.

REV. 0

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AD8512–SPECIFICATIONS (@ V_S = ±5 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)	V_{OS}			0.08	0.4	mV
		–40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)	V_{OS}			0.1	0.9	mV
		–40°C < T_A < +125°C			1.8	mV
Input Bias Current	I_B			21	75	pA
		–40°C < T_A < +85°C			0.7	nA
		–40°C < T_A < +125°C			7.5	nA
Input Offset Current	I_{OS}			5	50	pA
		–40°C < T_A < +85°C			3	nA
		–40°C < T_A < +125°C			5	nA
Input Voltage Range			–2.1		+2.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –2.1 V to +2.5 V	86	100		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ, V_O = –3 V to +3 V	65	107		V/mV
Offset Voltage Drift (B Grade)	$\Delta V_{OS}/\Delta T$			0.9	5	µV/°C
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			1.7	10	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ,	+4.1	+4.3		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–4.9	–4.7	V
Output Voltage High	V_{OH}	R_L = 2 kΩ,	+3.9	+4.2		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–4.9	–4.5	V
Output Voltage High	V_{OH}	R_L = 600 Ω,	+3.7	+4.1		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–4.8	–4.2	V
Output Current	I_{OUT}		±40	±54		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86	130		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.8	2.3	mA
		–40°C < T_A < +125°C			2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			8		MHz
Settling Time	t_S	To 0.1%, 0 V to 4 V Step, G = 1		0.4		µs
THD + Noise	THD + N	1 kHz, G = 1, R_L = 2 kΩ		0.0005		%
Phase Margin	Øo			44.5		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 Hz		34		nV/√Hz
	e_n	f = 100 Hz		12		nV/√Hz
	e_n	f = 1 kHz		8.0	10	nV/√Hz
	e_n	f = 10 kHz		7.6		nV/√Hz
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz Bandwidth		2.4	5.2	µV p-p

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade)	V_{OS}			0.08	0.4	mV
		–40°C < T_A < +125°C			0.8	mV
Offset Voltage (A Grade)	V_{OS}			0.1	1.0	mV
		–40°C < T_A < +125°C			1.8	mV
Input Bias Current	I_B			25	80	pA
		–40°C < T_A < +85°C			0.7	nA
		–40°C < T_A < +125°C			10	nA
Input Offset Current	I_{OS}			3.5	75	pA
		–40°C < T_A < +85°C			3	nA
		–40°C < T_A < +125°C			5	nA
Input Voltage Range			–13.5		+13.0	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –12.5 V to +12.5 V	86	108		dB
Large Signal Voltage Gain	A_{VO}	V_O = –13.5 V to +13.5 V R_L = 2 kΩ, V_{CM} = 0 V	115	196		V/mV
Offset Voltage Drift (B Grade)	$\Delta V_{OS}/\Delta T$			1.0	5	µV/°C
Offset Voltage Drift (A Grade)	$\Delta V_{OS}/\Delta T$			1.7	10	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 10 kΩ,	+14.0	+14.2		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–14.9	–14.6	V
Output Voltage High	V_{OH}	R_L = 2 kΩ,	+13.8	+14.1		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–14.8	–14.5	V
Output Voltage High	V_{OH}	R_L = 600 Ω,	+13.5	+13.8		V
Output Voltage Low	V_{OL}	–40°C < T_A < +125°C		–14.3	–13.8	V
Output Current	I_{OUT}			±45		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V	86			dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		1.9	2.3	mA
		–40°C < T_A < +125°C			2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		20		V/µs
Gain Bandwidth Product	GBP			8		MHz
Settling Time	t_S	To 0.1%, 0 V to 10 V Step, G = 1		0.5		µs
		To 0.01%, 0 V to 10 V Step, G = 1		0.9		µs
THD + Noise	THD + N	1 kHz, G = 1, R_L = 2 kΩ		0.0005		%
Phase Margin	Øo			52		Degrees
NOISE PERFORMANCE						
Voltage Noise Density	e_n	f = 10 Hz		34		nV/√Hz
	e_n	f = 100 Hz		12		nV/√Hz
	e_n	f = 1 kHz		8.0	10	nV/√Hz
	e_n	f = 10 kHz		7.6		nV/√Hz
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz Bandwidth		2.4	5.2	µV p-p

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±18 V
Input Voltage . . . . . $\pm V_S$
Output Short-Circuit Duration
to GND . . . . . Observe Derating Curves
Storage Temperature Range
R, RM Packages . . . . . –65°C to +150°C
Operating Temperature Range . . . . . –40°C to +125°C
Junction Temperature Range
R, RM Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C
Electrostatic Discharge (HBM) . . . . . 2000 V

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
8-Lead MSOP (RM)	210	45	°C/W
8-Lead SOIC (R)	158	43	°C/W

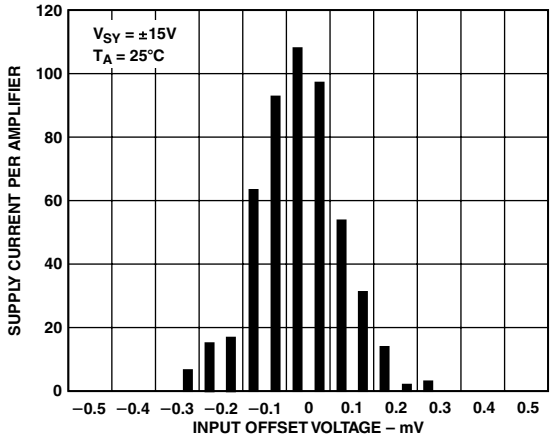
*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

ORDERING GUIDE

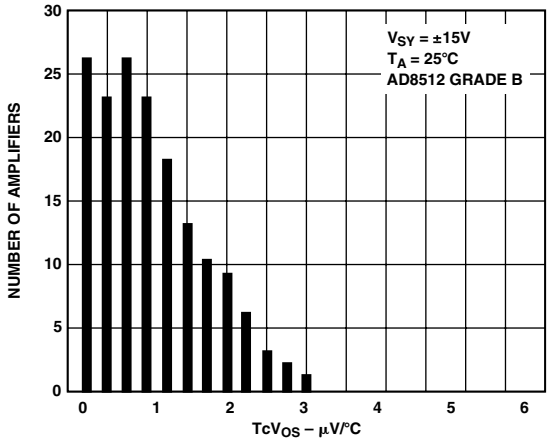
Model	Temperature Range	Package Description	Package Option	Branding Information
AD8512AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8512AR-Reel	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8512AR-Reel7	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8512ARM-Reel	–40°C to +125°C	8-Lead MSOP	RM-8	B8A
AD8512BR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8512BR-Reel	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8512BR-Reel7	–40°C to +125°C	8-Lead SOIC	SO-8	

CAUTION

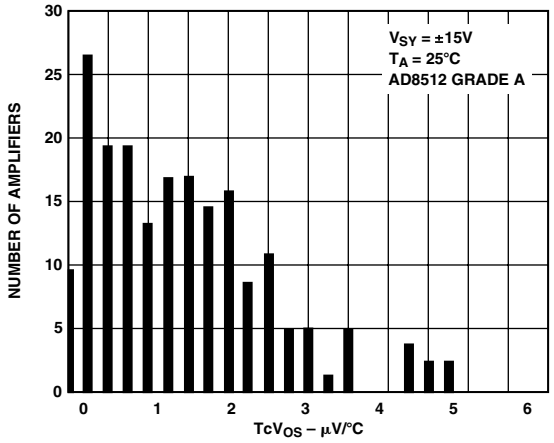
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8512 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



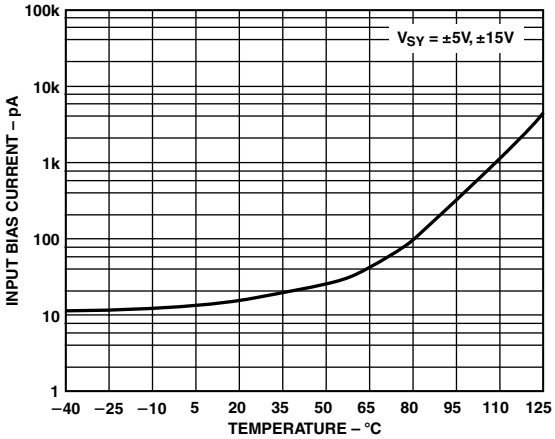
TPC 1. Input Offset Voltage Distribution



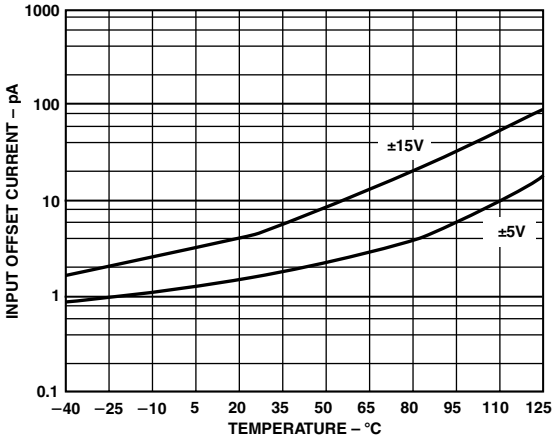
TPC 2. TcV_{OS} Distribution



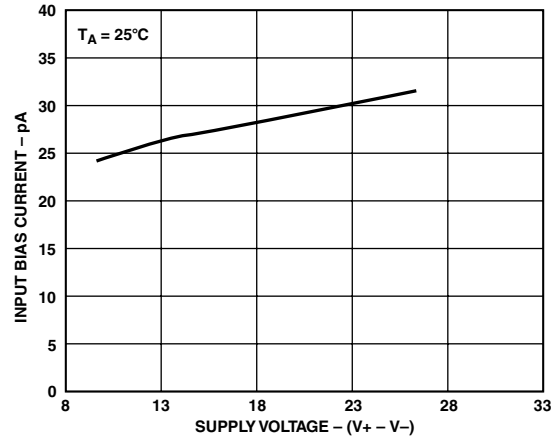
TPC 3. TcV_{OS} Distribution



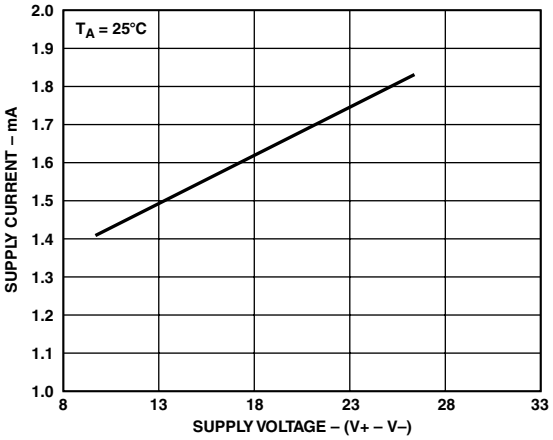
TPC 4. Input Bias Current vs. Temperature



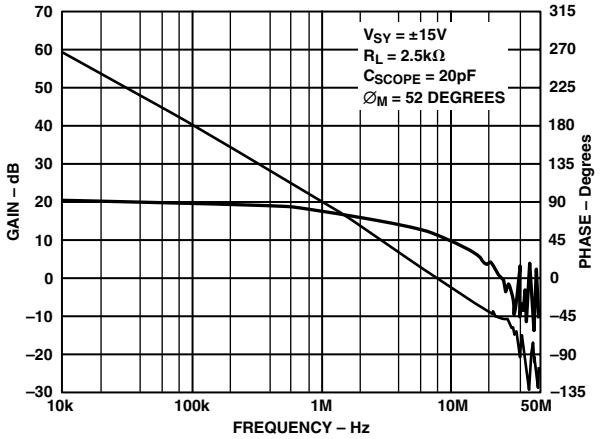
TPC 5. Input Offset Current vs. Temperature



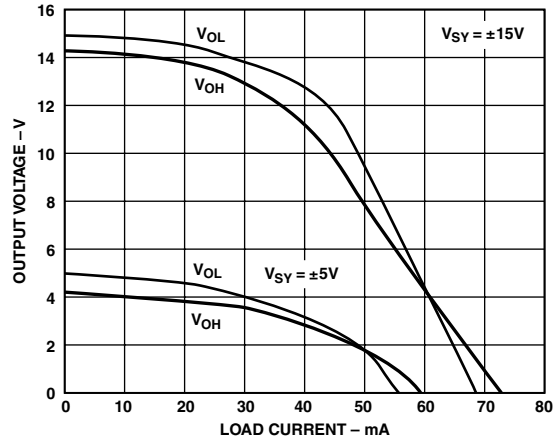
TPC 6. Input Bias Current vs. Supply Voltage



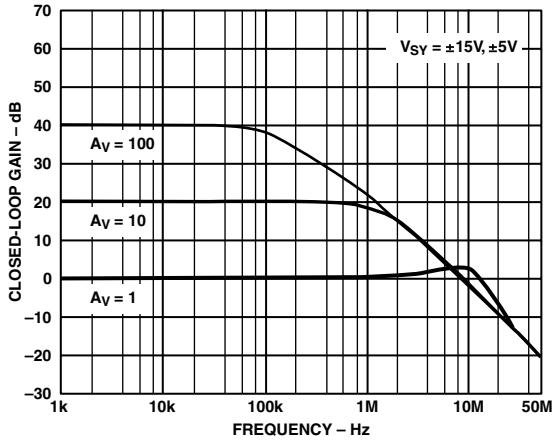
TPC 7. Supply Current/Amplifier vs. Supply Voltage



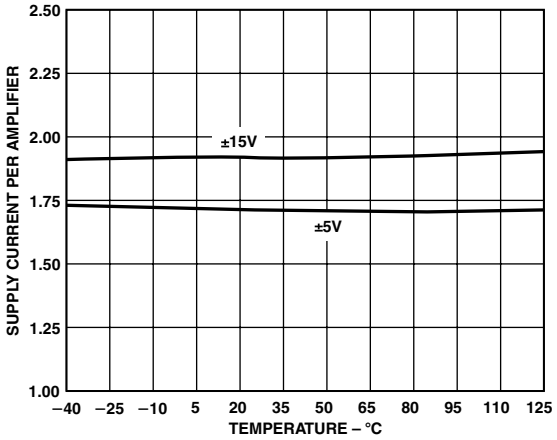
TPC 10. Open-Loop Gain and Phase vs. Frequency



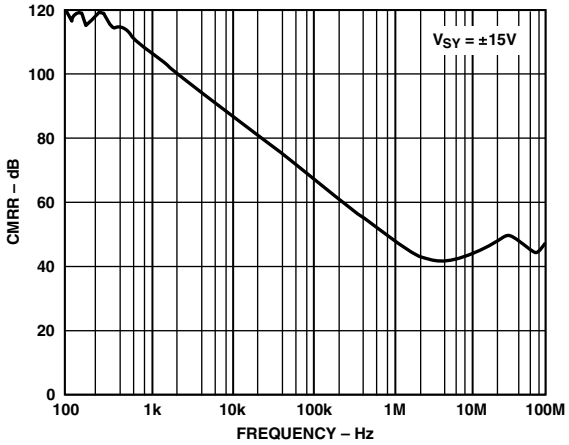
TPC 8. Output Voltage vs. Load Current



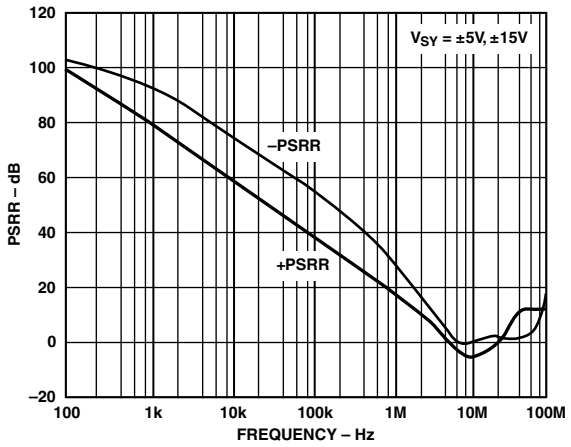
TPC 11. Closed-Loop Gain vs. Frequency



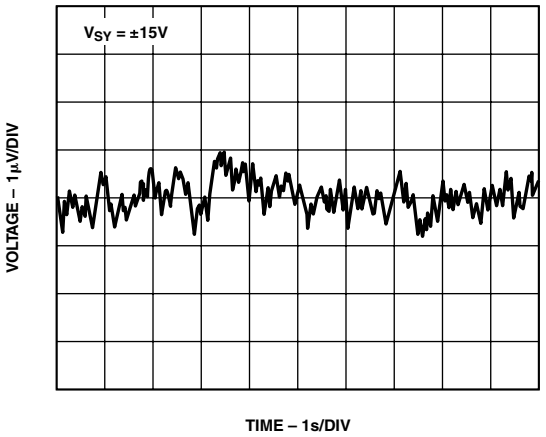
TPC 9. Supply Current/Amplifier vs. Temperature



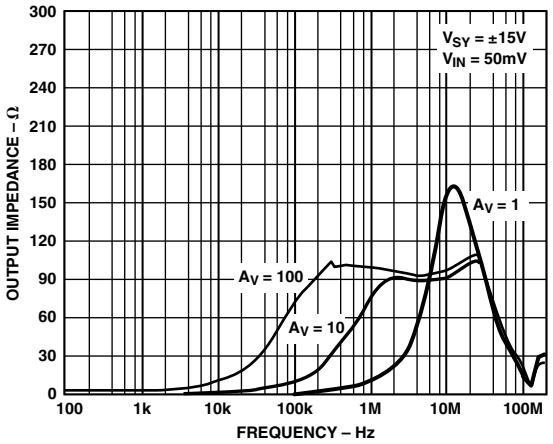
TPC 12. CMRR vs. Frequency



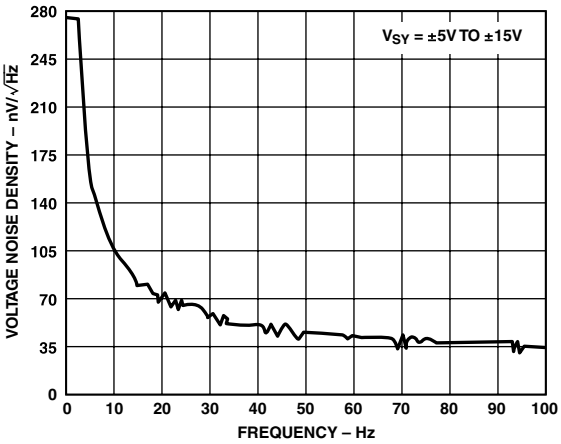
TPC 13. PSRR vs. Frequency



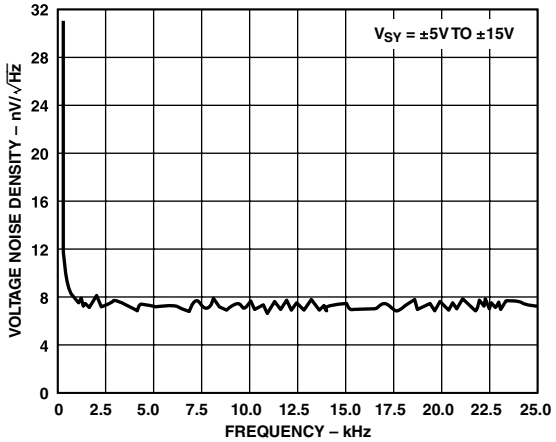
TPC 16. 0.1 Hz to 10 Hz Input Voltage Noise



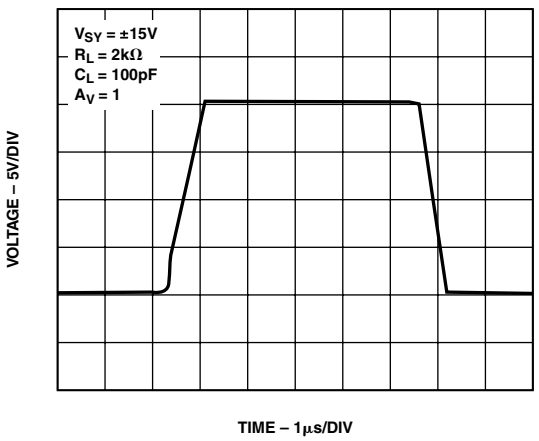
TPC 14. Output Impedance vs. Frequency



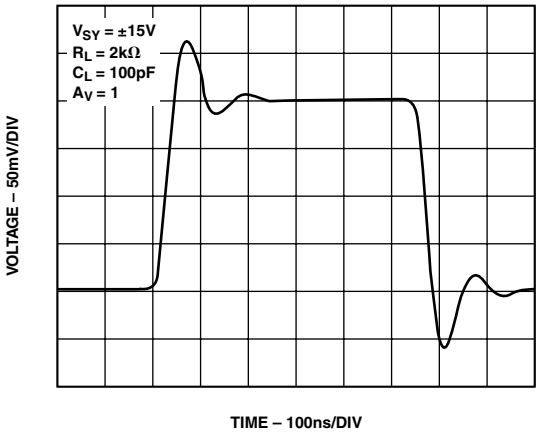
TPC 17. Voltage Noise Density



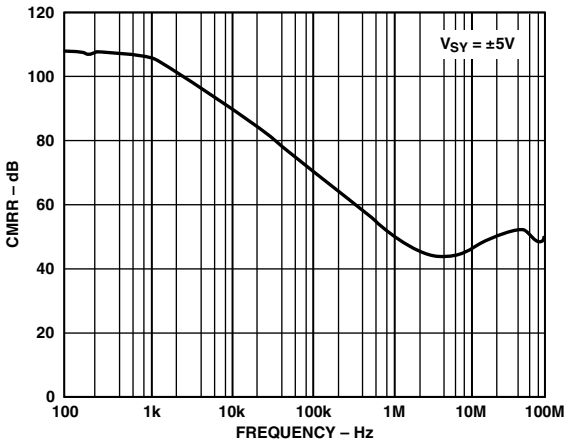
TPC 15. Voltage Noise Density



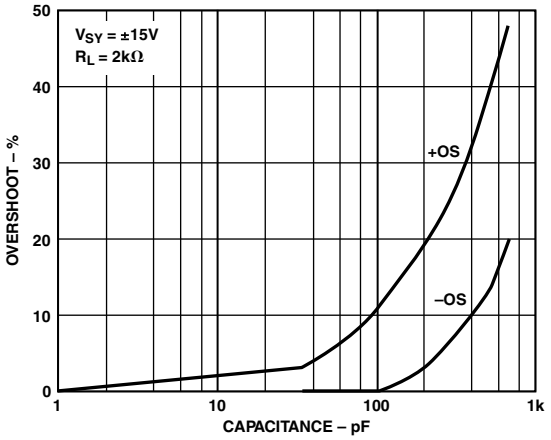
TPC 18. Large Signal Transient Response



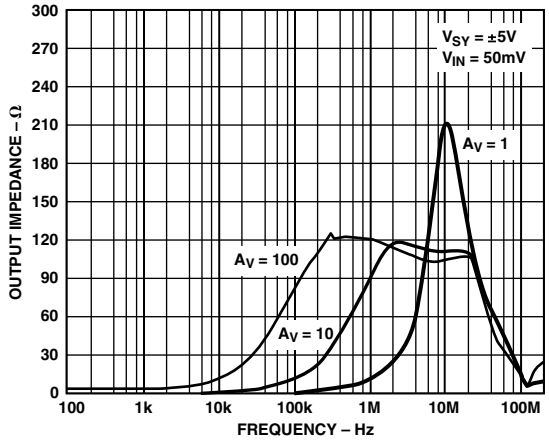
TPC 19. Small Signal Transient Response



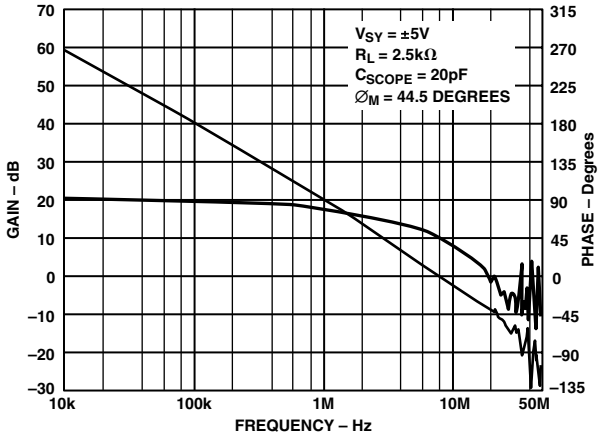
TPC 22. CMRR vs. Frequency



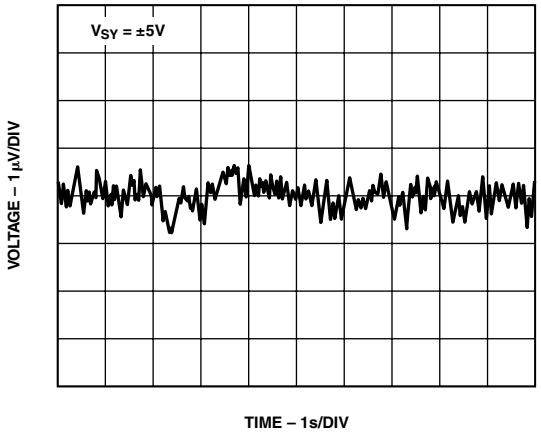
TPC 20. Small Signal Overshoot vs. Load Capacitance



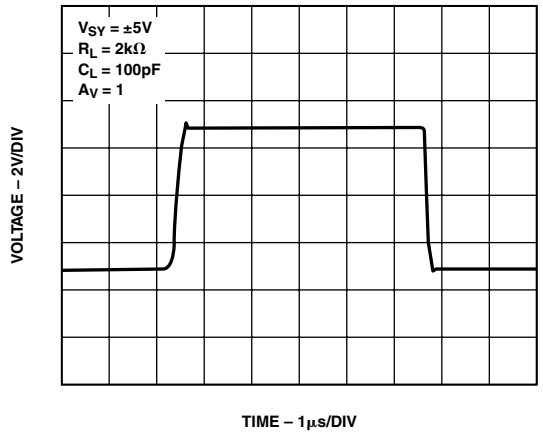
TPC 23. Output Impedance vs. Frequency



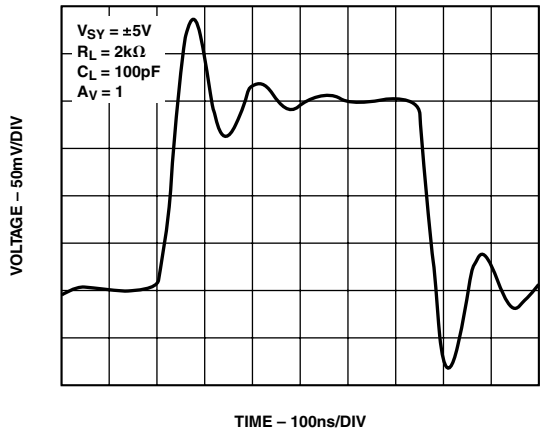
TPC 21. Open-Loop Gain and Phase vs. Frequency



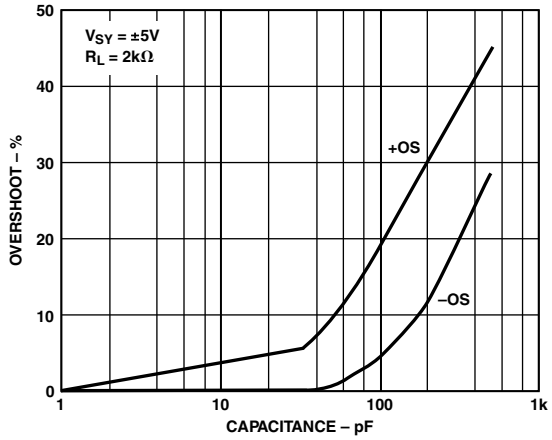
TPC 24. 0.1 Hz to 10 Hz Input Voltage Noise



TPC 25. Large Signal Transient Response



TPC 26. Small Signal Transient Response



TPC 27. Small Signal Overshoot vs. Load Capacitance

GENERAL APPLICATION INFORMATION

Input Overvoltage Protection

The AD8512 has internal protective circuitry, which allows voltages as high as 1.4 V beyond the supplies to be applied at the input of either terminal without causing damage.

For higher input voltages a series resistor is necessary to limit the input current. The resistor value can be determined from the formula:

$$\frac{V_{IN} - V_S}{R_S} \leq 5mA$$

With a very low offset current of < 2 nA up to 125°C, higher resistor values can be used in series with the inputs. A 5 kΩ resistor will protect the inputs to voltages as high as 25 V beyond the supplies and will add less than 10 μV to the offset.

Output Phase Reversal

Phase reversal is defined as a change of polarity in the transfer function of the amplifier. This can occur when the voltage applied at the input of an amplifier exceeds the maximum common-mode voltage. Phase reversal can cause permanent damage to the device and may result in system lockups. The AD8512 does not exhibit phase reversal when input voltages are beyond the supplies.

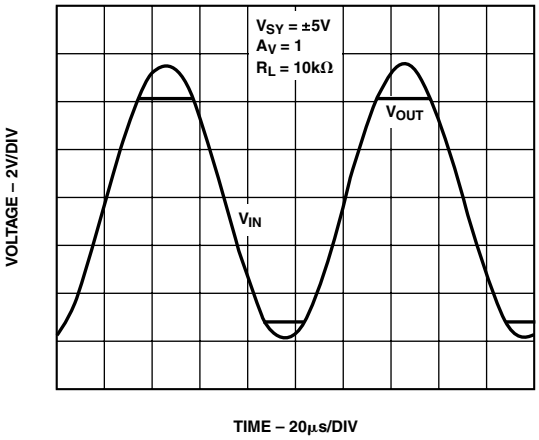


Figure 1. No Phase Reversal

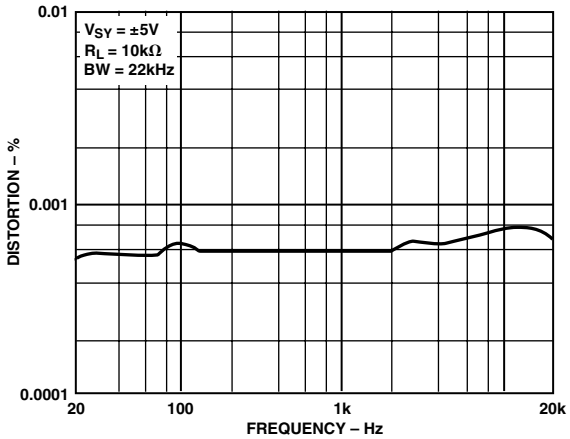


Figure 2. THD + N vs. Frequency

THD + Noise

The AD8512 has low total harmonic distortion and excellent gain linearity, which makes this amplifier a great choice for precision circuits with high closed-loop gain as well as audio application circuits.

Figure 2 shows that the AD8512 has approximately 0.0005% of total distortion when configured in positive unity gain (the worst case) and driving a 100 kΩ load.

Total Noise Including Source Resistors

The low input current noise and input bias current of the AD8512 make it the ideal amplifier for circuits with substantial input source resistance. Input offset voltage increases by less than 15 nV per 500 Ω of source resistance at room temperature.

The total noise density of the circuit is:

$$e_{nTOTAL} = \sqrt{e_n^{\,2} + \left(i_n R_S\right)^2 + 4kTR_S}$$

Where, e_n is the input voltage noise density of the AD8512
i_n is the input current noise density of the AD8512
R_S is the source resistance at the noninverting terminal
k is Boltzman's constant (1.38×10^{-23} J/K)
T is the ambient temperature in Kelvin (T = 273 + °C)

For R_S < 3.9 kΩ, e_n dominates and $e_{n,total} \approx e_n$

The current noise of the AD8512 is so low that its total density does not become a significant term unless R_S is greater than 165 MΩ, a value that is impractical for most applications.

The total equivalent rms noise over a specific bandwidth is expressed as:

$$e_{nTOTAL} = e_{nTOTAL}\sqrt{BW}$$

Where BW is the bandwidth in Hertz.

NOTE: The above analysis is valid for frequencies larger than 150 Hz and assumes flat noise, above 10 kHz. For lower frequencies, flicker noise (1/f) must be considered.

Settling Time

Settling time is defined as the time it takes the output of the amplifier to reach and remain within a percentage of its final value after a pulse has been applied at the input.

The AD8512 will settle to within 0.01% in less than 900 ns with a step of 0 V to 10 V in unity gain.

This makes it an excellent choice as a buffer at the output of DACs whose settling time is typically less than 1 μs.

In addition to its fast settling time and fast slew rate, the AD8512's low offset voltage drift and input offset current maintain full accuracy of 12-bit converters over the entire operating temperature range.

Overload Recovery Time

Overload recovery, also known as overdrive recovery, is the time it takes the output of an amplifier to recover from a saturated condition to its linear region. This recovery time is particularly important in applications where the amplifier must amplify small signals in the presence of large transient voltages.

Figure 3 shows the positive overload recovery of the AD8512. The output recovers in approximately 200 ns from a saturated condition.

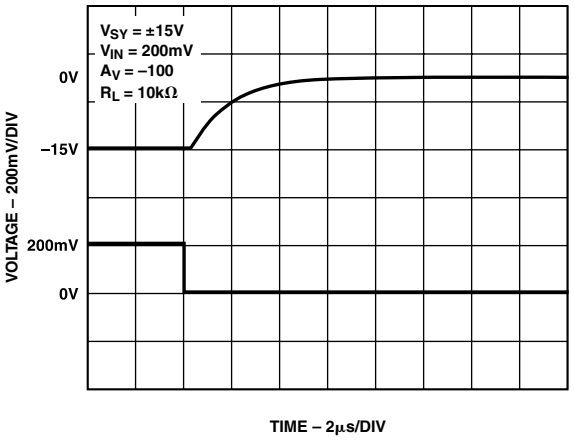


Figure 3. Positive Overload Recovery

The negative overdrive recovery time, Figure 4, is less than 200 ns.

In addition to the fast recovery time, the AD8512 shows excellent symmetry of the positive and negative recovery times. This is an important feature for transient signal rectification because the output signal is kept equally undistorted throughout any given period.

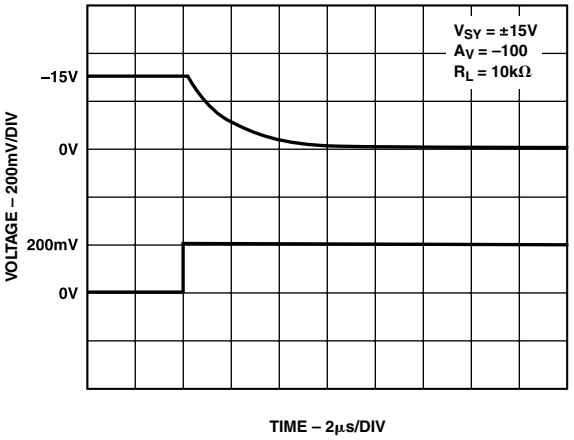


Figure 4. Negative Overload Recovery

Capacitive Load Drive

The AD8512 is unconditionally stable at all gains in inverting and noninverting configurations. It is capable of driving up to 1000 pF of capacitive loads without oscillation in unity gain, the worst-case configuration.

However, as with most amplifiers, driving larger capacitive loads in a unity gain configuration may cause excessive overshoot and ringing, or even oscillation.

A simple "snubber network" reduces the amount of overshoot and ringing significantly. The advantage of this configuration is that the output swing of the amplifier is not reduced because R_S is outside the feedback loop.

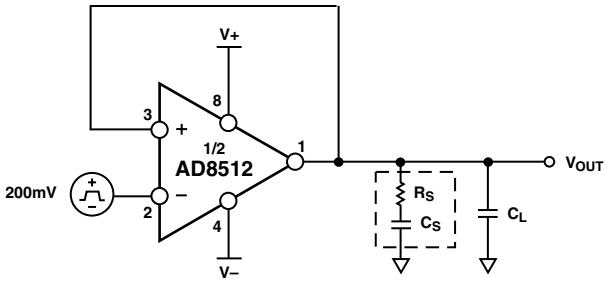


Figure 5. Snubber Network Configuration

Figure 6 shows a scope photograph of the output of the AD8512 in response to a 400 mV pulse. The circuit is configured in positive unity gain (worst case) with a load capacitance of 500 pF.

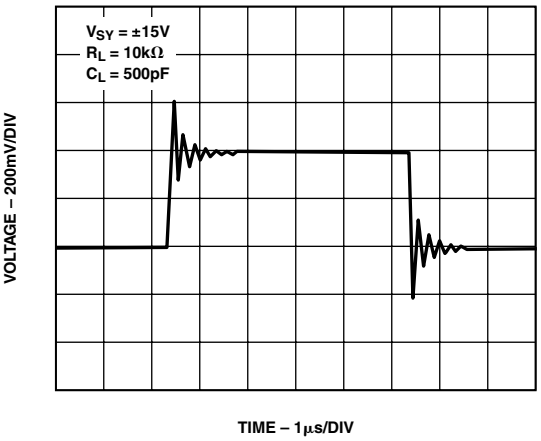


Figure 6. Capacitive Load Drive Without Snubber

When the "snubber" circuit is used, the overshoot is reduced from 55% to less than 3% with the same load capacitance. Ringing is virtually eliminated as shown in Figure 7.

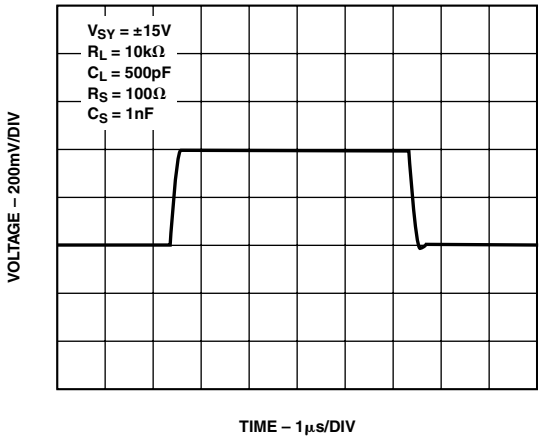


Figure 7. Capacitive Load With Snubber Network

Optimum values for R_S and C_S depend on the load capacitance and input stray capacitance and are determined empirically. Table I shows a few values that can be used as starting points.

Table I. Optimum Values for Capacitive Loads

C_{LOAD}	R_S (Ω)	C_S
500 pF	100	1 nF
2 nF	70	100 pF
5 nF	60	300 pF

Open-Loop Gain and Phase Response

In addition to its impressive low noise, low offset voltage and offset current, the AD8512 has excellent loop gain and phase response even when driving large resistive and capacitive loads.

It was compared to the OPA2132 under the same conditions. With a 2.5 kΩ load at the output, the AD8512 has over 8 MHz of bandwidth and a phase margin of more than 52°.

The OPA2132, on the other hand, has only 4.5 MHz of bandwidth and 28° of phase margin under the same test conditions.

Even with a 1 nF capacitive load in parallel with the 2 kΩ load at the output, the AD8512 shows much better response than the OPA2132, whose phase margin is degraded to less than 0, indicating oscillation.

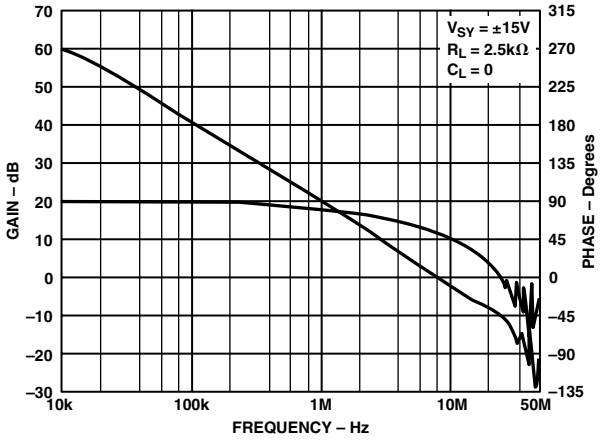


Figure 8. Frequency Response of the AD8512

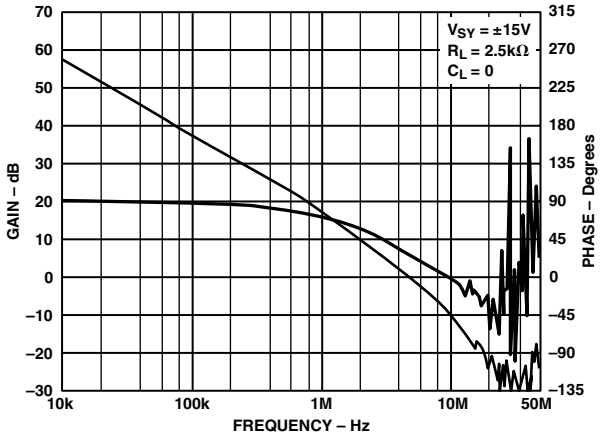


Figure 9. Frequency Response of the OPA2132

Precision Rectifiers

Rectifying circuits are used in a multitude of applications. One of the most popular uses is in the design of regulated power supplies where a rectifier circuit is used to convert an input sinusoid to a unipolar output voltage. There are some potential problems for amplifiers used in this manner.

When the input voltage (Vi) is negative, the output is zero. The magnitude of Vi is doubled at the inputs of the op amp. This voltage can exceed the power supply voltage. This would damage some amplifiers permanently. The op amp must come out of saturation when Vi is negative. This delays the output signal, as the amplifier requires time to enter its linear region.

The AD8512 has a very fast overdrive recovery time, which makes it a great choice for the rectification of transient signals. The symmetry of the positive and negative recovery times is also important in keeping the output signal undistorted.

Figure 10 shows the test circuit of the rectifier. The first stage of the circuit is a half wave rectifier. When the sine wave applied at the input is positive, the output follows the input response. During the negative cycle of the input, the output tries to swing negative to follow the input but the power supply restrains it to zero.

In a similar fashion, the second stage is a follower during the positive cycle of the sine wave and an inverter during the negative cycle.

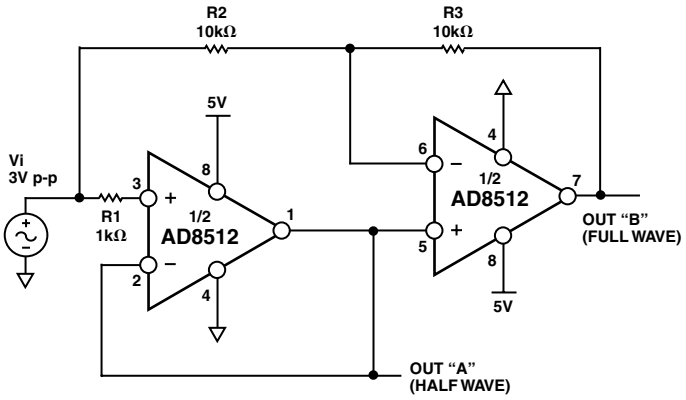


Figure 10. Half Wave and Full Wave Rectifier

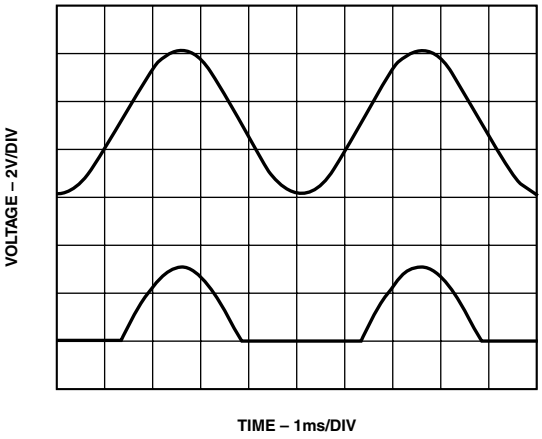


Figure 11. Half Wave Rectified Signal (Out A)

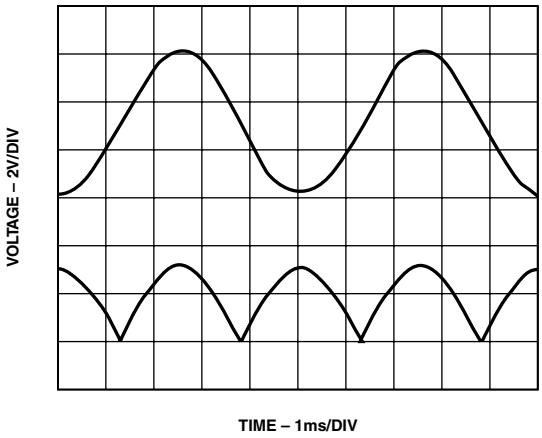


Figure 12. Full Wave Rectified Signal (Out B)

I-V CONVERSION APPLICATIONS

Photodiode Circuits

Common applications for I-V conversion include photodiode circuits where the amplifier is used to convert a current emitted by a diode placed at the positive input terminal into an output voltage.

The AD8512 low input bias current, wide bandwidth, and low noise make it an excellent choice for various photodiode applications including fax machines, fiber optic controls, motion sensors, and bar code readers.

The circuit shown in Figure 13 uses a silicon diode with zero bias voltage. This is known as a photovoltaic mode; this configuration limits the overall noise and is suitable for instrumentation applications.

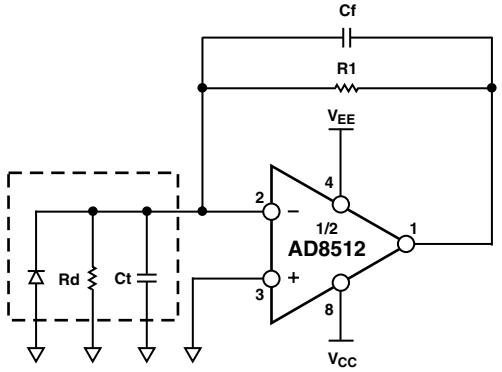


Figure 13. Equivalent Preamplifier Photodiode Circuit

A larger signal bandwidth can be attained at the expense of additional output noise. The total input (Ct) capacitance consists of the sum of the diode capacitance (typically 3 pF to 4 pF) and the amplifier's input capacitance (12 pF), which includes external parasitic capacitance. Ct creates a pole in the frequency response, which may lead to an unstable system. To ensure stability and optimize the bandwidth of the signal, a capacitor is placed in the feedback loop of the circuit shown in Figure 13. It creates a zero and yields a bandwidth whose frequency is 1/(2(R1Cf)).

The value of R1 can be determined by the ratio V/I_D, where V is the desired output voltage of the op amp and I_D the diode current. For example, if I_D is 100 μA, and the output voltage that is desired is 10 V, then R1 should be 100 kΩ. Rd is a junction resistance, which drops typically by a factor of 2 for every 10°C increase in temperature. A typical value for Rd is 1000 MΩ. Since Rd is >> R1, the circuit behavior is not impacted by the effect of the junction resistance. The maximum signal bandwidth is:

$$f_{MAX} = \sqrt{\frac{ft}{2\pi R2Ct}}$$

where *ft* is the unity gain frequency of the amplifier.

Using the parameters of the example above Cf ≈ 1 pF. This yields a signal bandwidth of about 2.6 MHz.

$$Cf = \sqrt{\frac{Ct}{2\pi R2\,ft}}$$

where *ft* is the unity gain frequency of the op amp, achieves a phase margin Fm of approximately 45°.

A higher phase margin can be obtained by increasing the value of Cf. Setting Cf to twice the previous value yields approximately Fm = 65° and a maximally flat frequency response. This comes at a cost of 50% reduction in the maximum signal bandwidth.

Signal Transmission Applications

One popular signal transmission method uses pulsewidth modulation. High data rates may require a fast comparator rather than an op amp. However, the need for sharp and undistorted signals may favor using a linear amplifier.

The AD8512 makes an excellent voltage comparator. In addition to its high slew rate, the AD8512 has a very fast saturation recovery time. In the absence of feedback, the amplifier is in open-loop mode (very high gain). In this mode of operation it spends much of its time in saturation.

The circuit of Figure 14 compares two signals of different frequencies, namely a sine wave of 100 Hz and a triangular wave of 1 kHz. Figure 15 shows a scope photograph of the output waveform. A pull-up resistor (typically 5 kΩ) may be connected from the output to V_{CC} if the output voltage needs to reach the positive rail. The trade-off is that power consumption will be higher.

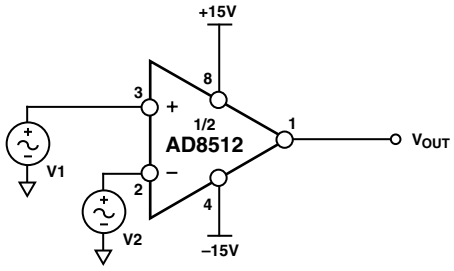


Figure 14. Pulsewidth Modulator

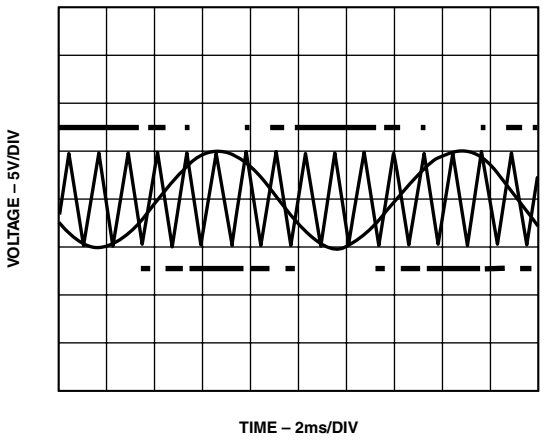


Figure 15. Pulsewidth Modulation

Cross Talk

Cross talk, also known as channel separation, is a measure of signal feedthrough from one channel to the other on the same IC.

The AD8512 has a channel separation greater than –140 dB for frequencies up to 20 kHz and greater than –130 dB for frequencies up to 10 MHz.

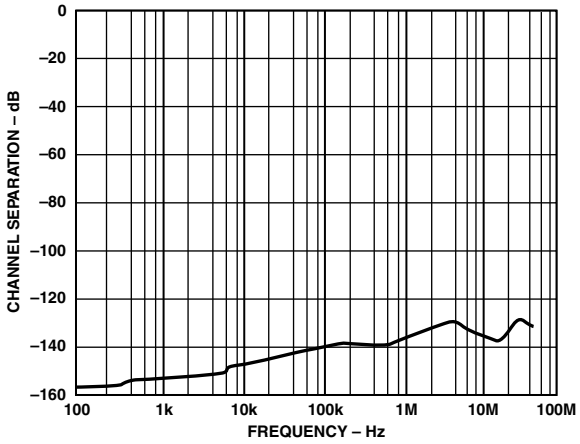


Figure 16. Channel Separation

Precision Current Monitoring

The low offset voltage and input bias current of the AD8512 make it an excellent choice for precision current sensing applications.

The circuit of Figure 17 shows a low side current monitor. R_{SENSE} creates a voltage drop across it that is proportional to the load current. This voltage appears at the inverting node of the op amp and creates a current through R2.

The equation for the output voltage is written:

$$V_{OUT} = \left(\frac{I_L \times R_{SENSE}}{R_1} \right) \times R2$$

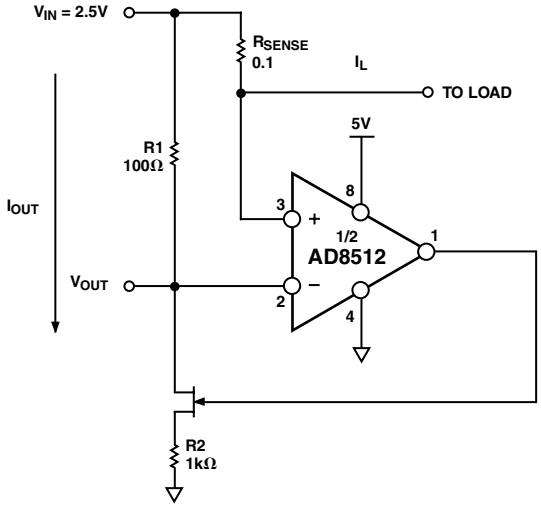
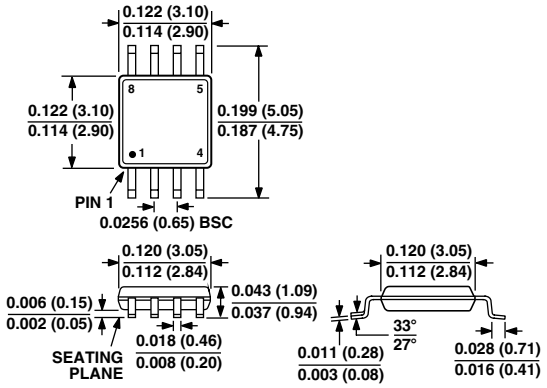


Figure 17. High Side Current Monitor

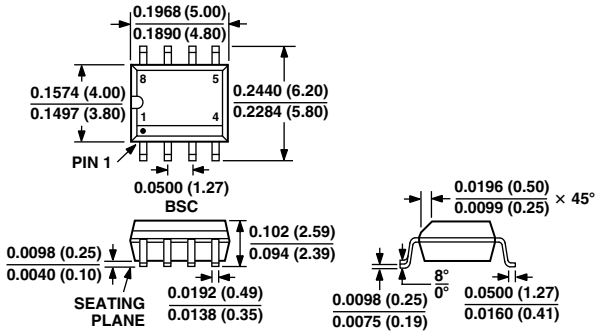
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead MSOP
(RM Suffix)



8-Lead SOIC
(R Suffix)



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