

Smart High-Side Power Switch

Two Channels: 2 x 100mΩ

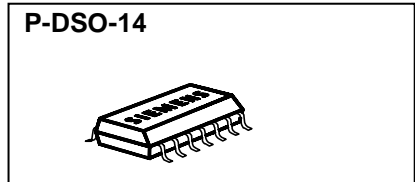
Status Feedback

Suitable for 42V

Product Summary

Operating Voltage	$V_{bb(on)}$	7.0 ... 58V	
	Active channels	One	two parallel
On-state Resistance	R_{ON}	105mΩ	53mΩ
Nominal load current	$I_{L(NOM)}$	2.9A	4.2A
Current limitation	$I_{L(SCr)}$	8A	8A

Package



General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® 80V technology.
- Providing embedded protective functions
- An array of resistors is integrated in order to reduce the external components

Applications

- μ C compatible high-side power switch with diagnostic feedback for 12V and 24V and **42V** grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for inductive loads
- Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

- CMOS compatible input
- Improved electromagnetic compatibility (EMC)
- Fast demagnetization of inductive loads
- Stable behaviour at undervoltage
- Wide operating voltage range
- Logic ground independent from load ground
- Optimized inverscurrent capability

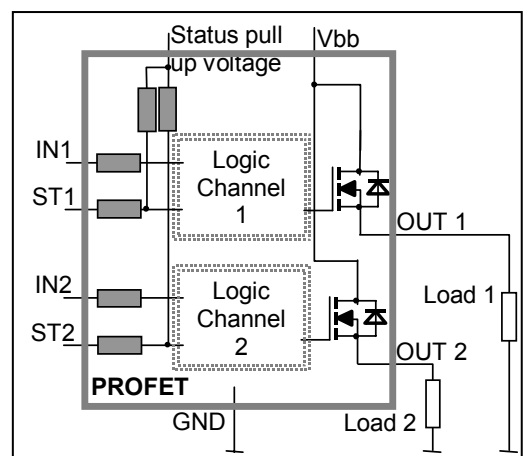
Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

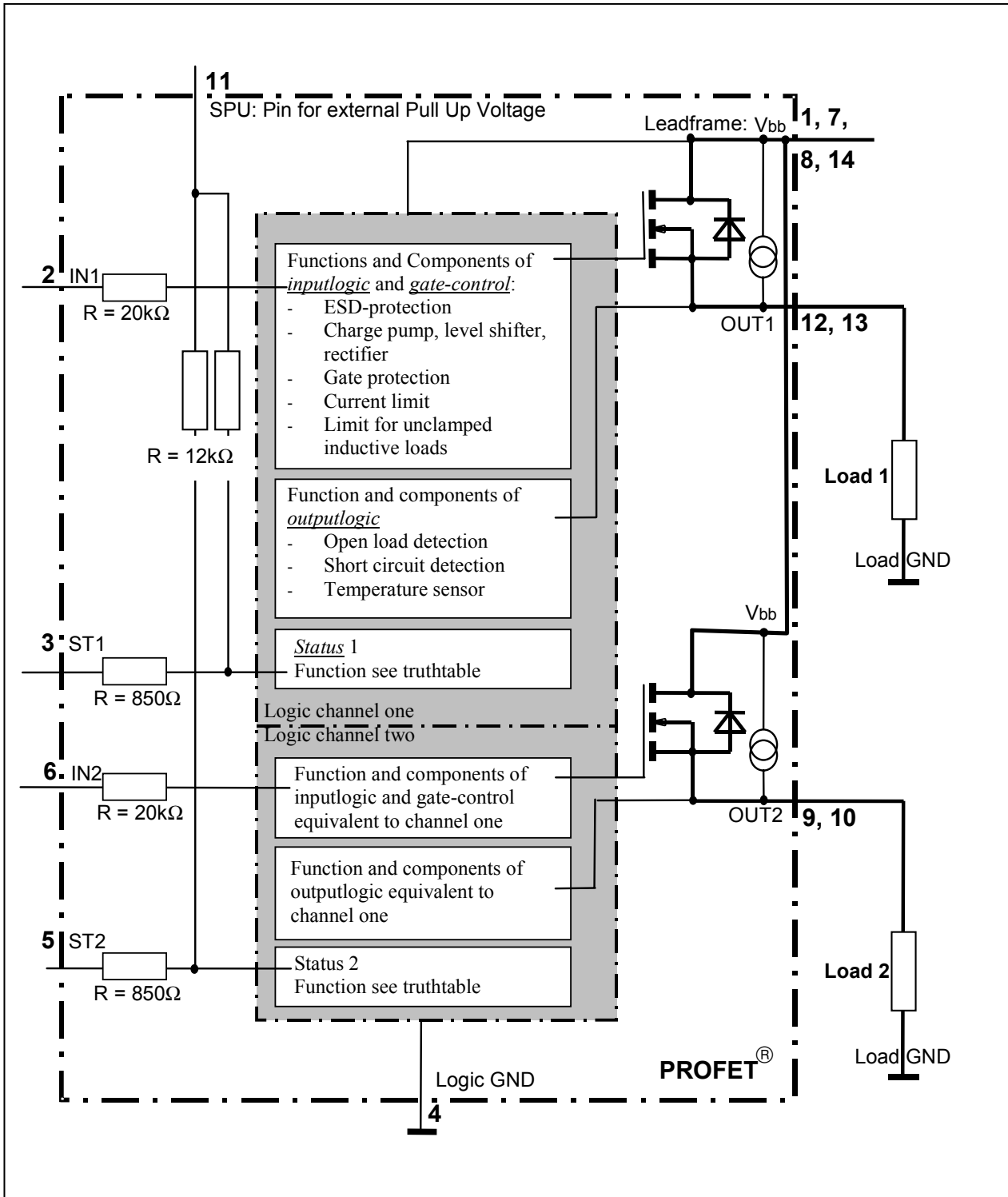
Diagnostic Function

- Diagnostic feedback with open drain output and integrated pull up resistors
- Open load detection in OFF-state
- Feedback of thermal shutdown in ON-state
- Diagnostic feedback of both channels works properly in case of inverse current

Block Diagram



Functional diagram

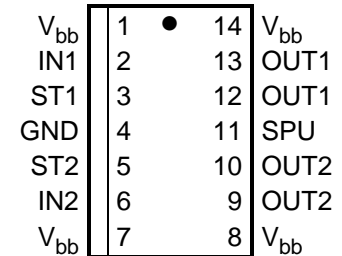


Pin Definitions and Functions

Pin	Symbol	Function
1,7, 8,14,	V_{bb}	Positive power supply voltage. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
2	IN1	Input 1,2 activates channel 1,2 in case of logic high signal
6	IN2	
12,13	OUT1	Output 1,2 protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current; both outputpins have to be connected in parallel for operation according this spec.
9,10	OUT2	
3	ST1	Diagnostic feedback 1,2 of channel 1,2 open drain
5	ST2	
4	GND	Logic Ground
11	SPU	Connection for external pull up voltage source for the open drain status output. Pull up resistors are integrated.

Pin configuration

(top view)



Maximum Ratings at $T_j = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Values	Unit
Supply voltage (overvoltage protection see page 6)	V_{bb}	58	V
Supply voltage for full short circuit protection $T_{j,start} = -40 \dots +150^\circ\text{C}$	V_{bb}	50	V
Output Voltage to V_{bb}	V_{ON}	70	V
Negative voltage slope at output	$-dV_{OUT}/dt$	20	V/ μs
Load current (Short-circuit current, see page 7)	I_L	$I_{L(LIM)}^{1)}$	A
Load dump protection ²⁾ $V_{LoadDump} = V_A + V_s$, $V_A = 27\text{ V}$ $R_l^{3)} = 8\ \Omega$, $t_d = 200\text{ ms}$; IN = low or high, each channel loaded with $R_L = 20\ \Omega$,	$V_{Load\ dump}^{4)}$	70	V
Operating temperature range	T_j	-40 ... +150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 ... +150	
Power dissipation (DC) ⁵⁾ (all channels active)	P_{tot}	$T_a = 25^\circ\text{C}$: 3.0 $T_a = 85^\circ\text{C}$: 1.6	W
Maximal switchable inductance, single pulse $V_{bb} = 12\text{V}$, $T_{j,start} = 150^\circ\text{C}^{5)}$, $I_L = 2.5\text{ A}$, $E_{AS} = 110\text{ mJ}$, $0\ \Omega$ one channel: $I_L = 3.5\text{ A}$, $E_{AS} = 278\text{ mJ}$, $0\ \Omega$ two parallel channels: see diagrams on page 12	Z_L	23.0 30.0	mH
Electrostatic discharge capability (ESD): (Human Body Model) acc. MIL-STD883D, method 3015.7 and ESD assn. std. S5.1-1993 $R=1.5\text{k}\Omega$; $C=100\text{pF}$	V_{ESD}	1.0	kV
Input voltage (DC)	V_{IN}	± 42	V
Current through input pin (DC)	I_{IN}	± 2.0	mA
Current through status pin (DC)	I_{ST}	± 2.0	
Status pull up voltage	V_{SPU}	± 42	V

1) Current limit is a protection function. Operation in current limitation is considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

2) Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GND and status pins (a 150 Ω resistor for the GND connection is recommended).

3) R_l = internal resistance of the load dump test pulse generator

4) $V_{Load\ dump}$ is setup without the DUT connected to the generator per ISO 7637-1 and DIN 40839

5) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

Thermal Characteristics

Parameter and Conditions	Symbol	Values			Unit
		min	typ	Max	
Thermal resistance junction - soldering point ^{5),6)} each channel:	R_{thjs}	--	--	25	K/W
junction - ambient ⁵⁾ one channel active:	R_{thja}	--	45	--	
all channels active:		--	41	--	

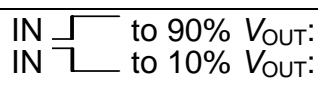
Electrical Characteristics

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 24\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

Load Switching Capabilities and Characteristics

On-state resistance (V_{bb} to OUT); $I_L = 2\text{ A}$, $V_{bb} \geq 7\text{ V}$ each channel, $T_j = 25^\circ\text{C}$: $T_j = 150^\circ\text{C}$: two parallel channels, $T_j = 25^\circ\text{C}$: see diagram, page 12	R_{ON}	--	90 170 45	105 210 53	$\text{m}\Omega$
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⁶⁾ Soldering point: Upper side of solder edge of device pin 15. See page 15

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 24\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	
Nominal load current one channel active: two parallel channels active: Device on PCB ⁷⁾ , $T_a = 85^\circ\text{C}$, $T_j \leq 150^\circ\text{C}$	$I_{L(\text{NOM})}$	2.5 4.0	2.9 4.2	-- --	A
Output current while GND disconnected or pulled up ⁸⁾ ; $V_{bb} = 30\text{ V}$, $V_{IN} = 0$, see diagram page 11	$I_{L(\text{GNDhigh})}$	--	--	1.0	mA
Turn-on time ⁹⁾ Turn-off time $R_L = 12\ \Omega$	IN  to 90% V_{OUT} : to 10% V_{OUT} : t_{on} t_{off}	-- --	-- --	55 95	μs
Slew rate on ⁹⁾ 10 to 30% V_{OUT} , $R_L = 12\ \Omega$:	dV/dt_{on}	1.0	--	5	$\text{V}/\mu\text{s}$
Slew rate off ⁹⁾ 70 to 40% V_{OUT} , $R_L = 12\ \Omega$:	$-dV/dt_{\text{off}}$	1.0	--	5	$\text{V}/\mu\text{s}$

Operating Parameters

Operating voltage	$V_{bb(\text{on})}$	7.0	--	58	V
Undervoltage restart of charge pump $T_j = -40\dots+25^\circ\text{C}$: $T_j = +150^\circ\text{C}$:	$V_{bb(\text{ucp})}$	-- --	4 --	5.5 7.0	V
Overvoltage protection ¹⁰⁾ $I_{bb} = 40\text{ mA}$	$V_{bb(\text{AZ})}$	58.5	63	69	V
Standby current ¹¹⁾ $V_{IN} = 0$; see diagram page 10	$T_j = -40^\circ\text{C}\dots+25^\circ\text{C}$: $T_j = +125^\circ\text{C}$ ¹²⁾ : $T_j = +150^\circ\text{C}$:	$I_{bb(\text{off})}$	-- -- --	13 23 25	23 35 μA
Off-State output current (included in $I_{bb(\text{off})}$) $V_{IN} = 0$; each channel	$I_{L(\text{off})}$	--	3	--	μA
Operating current ¹³⁾ , $V_{IN} = 5\text{V}$, one channel on: all channels on:	I_{GND}	-- --	1.0 2.0	1.5 3.0	mA

7) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for V_{bb} connection. PCB is vertical without blown air. See page 15

8) not subject to production test, specified by design

9) See timing diagram on page 13.

10) Supply voltages higher than $V_{bb(\text{AZ})}$ require an external current limit for the GND; a 150 Ω resistor is recommended. See also $V_{\text{ON}(\text{CL})}$ in table of protection functions and circuit diagram on page 10.

11) Measured with load; for the whole device; all channels off

12) not subject to production test, specified by design

13) Add I_{ST} , if $I_{\text{ST}} > 0$

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 24\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

Protection Functions¹⁴⁾

Current limit, (see timing diagrams, page 13)	$I_{L(\text{lim})}$				A
$T_j = -40^\circ\text{C}$:		--	10	12	
$T_j = 25^\circ\text{C}$:		--	9	--	
$T_j = +150^\circ\text{C}$:		5	8	--	
Repetitive short circuit current limit ¹⁵⁾ , $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 13)	$I_{L(\text{SCR})}$	--	8	--	A
		--	8	--	
Initial short circuit shutdown time $T_{j,\text{start}} = 25^\circ\text{C}$: (see timing diagrams on page 13)	$t_{\text{off}(\text{SC})}$	--	2	--	ms
Output clamp (inductive load switch off) ¹⁶⁾ at $V_{\text{ON}(\text{CL})} = V_{bb} - V_{\text{OUT}}$, $I_L = 1\text{ A}$	$V_{\text{ON}(\text{CL})}$	59	64	70	V
Thermal overload trip temperature	T_{jt}	150	--	--	$^\circ\text{C}$
Thermal hysteresis	ΔT_{jt}	--	10	--	K

Reverse Battery

Reverse battery voltage ¹⁷⁾	$-V_{bb}$	--	--	24	V
Drain-source diode voltage ($V_{\text{out}} > V_{bb}$) ¹⁸⁾ $I_L = -3.0\text{ A}$, $T_j = +150^\circ\text{C}$	$-V_{\text{ON}}$	--	650	--	mV

Inverse current ¹⁹⁾

GND current in case of 3A inverse current ²⁰⁾	$I_{\text{GND}(\text{inv cur})}$	--	--	15	mA
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¹⁴⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

¹⁵⁾ not subject to production test, specified by design

¹⁶⁾ If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{\text{ON}(\text{CL})}$

¹⁷⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 4 and circuit page 10).

¹⁸⁾ not subject to production test, specified by design

¹⁹⁾ not subject to production test, specified by design



²⁰⁾ In case of an inverse current of 3A the both status outputs must not be disturbed.
The neighbour channel can be switched normally; not all parameters lay within the range of the spec
Please note, that in case of an inverse current no protection function is active. The power dissipation is higher compared to normal operation in forward mode due to the voltage drop across the drain-source diode (as it is with reverse polarity). If this mode lasts for a too long time the device can be destroyed.

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 24\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

Diagnostic Characteristics

Open load detection current ²¹⁾	$I_{L(\text{off})}$	--	3	--	μA
Open load detection voltage	$V_{\text{OUT}(\text{OL})}$	2.0	2.85	3.7	V
Short circuit detection voltage ²²⁾ V_{bb} (pin 1,7,8,14) to OUT1 (pin 12,13) resp. V_{bb} (pin 1,7,8,14) to OUT2 (pin 9,10)	$V_{\text{ON}(\text{SC})}$	--	4.0	--	V

Input and Status Feedback ²³⁾

Integrated resistors; $T_j = 25^\circ\text{C}$: (see circuit page 2)	Input	R_i	--	20	--	$\text{k}\Omega$
	Status	R_{ST}	0.53	0.85	1.2	$\text{k}\Omega$
	Status pull up	$R_{\text{pull up}}$	--	12	--	$\text{k}\Omega$
Input turn-on threshold voltage		$V_{\text{IN}(\text{T}+)}$	1.2	--	2.2	V
Input turn-off threshold voltage		$V_{\text{IN}(\text{T}-)}$	1.0	--	--	V
Input threshold hysteresis		$\Delta V_{\text{IN}(\text{T})}$	--	0.25	--	V
Off state input current	$V_{\text{IN}} = 0.4\text{ V}$:	$I_{\text{IN}(\text{off})}$	1	--	15	μA
On state input current	$V_{\text{IN}} = 5\text{ V}$:	$I_{\text{IN}(\text{on})}$	10	25	50	μA
Status output (open drain)						
Zener limit voltage		$V_{\text{ST}(\text{high})}$	5.4	6.1	--	V
Status low voltage	$V_{\text{SPU}} = 5\text{ V}$:	$V_{\text{ST}(\text{low})}$	--	--	0.4	

²¹⁾ not subject to production test, specified by design

²²⁾ not subject to production test, specified by design

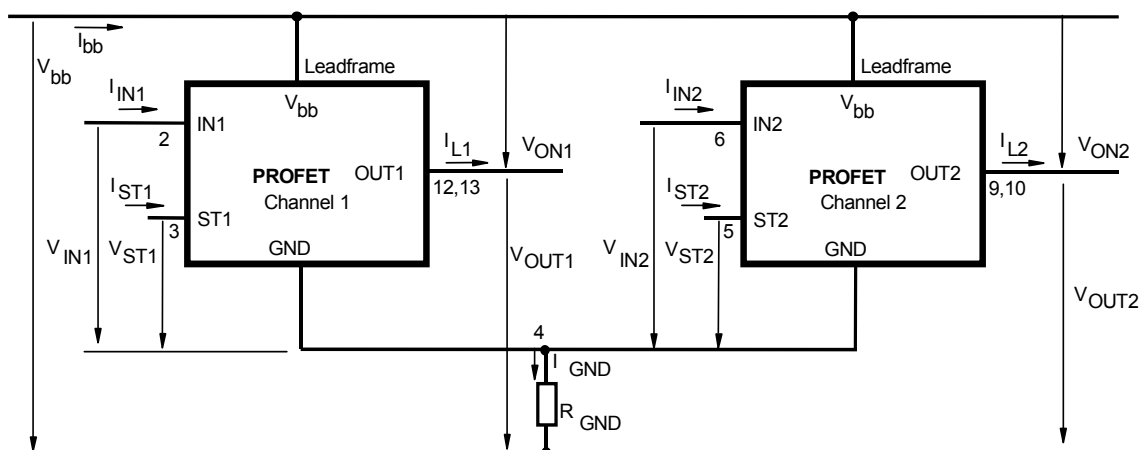
²³⁾ If a ground resistor R_{GND} is used, add the voltage drop across these resistors.

Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 723
Normal operation	L	L	L
	H	H	H
Open load	L	$V_{OUT} > 2.7V$	H
	H	H	H
Short circuit to GND	L	L	L
	H	L	L
Short circuit to V_{bb}	L	H	H
	H	H	H
Overtemperature	L	L	L
	H	L	L

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. In this mode it is recommended to use only one status.

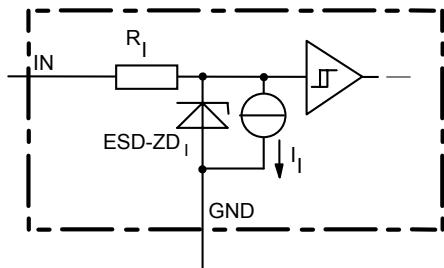
Terms



Leadframe (V_{bb}) is connected to pin **1,7,8,14**

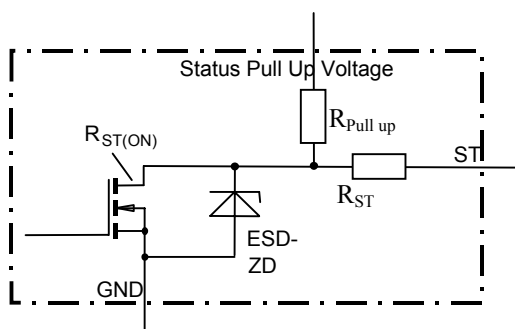
External R_{GND} optional; a single resistor $R_{GND} = 150\Omega$ for reverse battery protection up to the max. operating voltage.

Input circuit (ESD protection), IN1 or IN2



The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

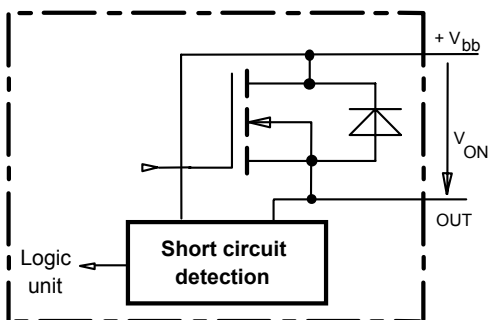
Status output, ST1 or ST2



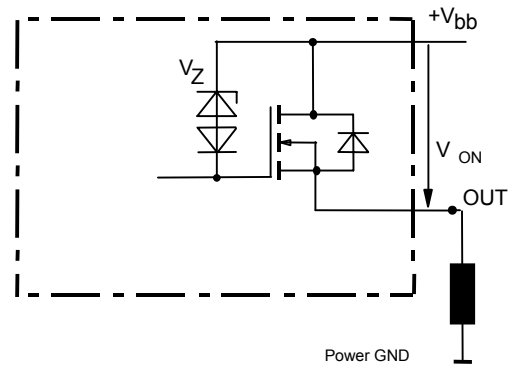
ESD-Zener diode: 6.1 V typ., $R_{ST(ON)} < 250 \Omega$,
 $R_{ST} = 850 \Omega$ typ., $R_{pull\ up} = 12\ k\Omega$ typ.
 The use of ESD zener diodes as voltage clamp at DC conditions is not recommended

Short Circuit detection

Fault Signal at ST-Pin: $V_{ON} > 4.0\ V$ typ, no switch off by the PROFET itself, external switch off recommended!

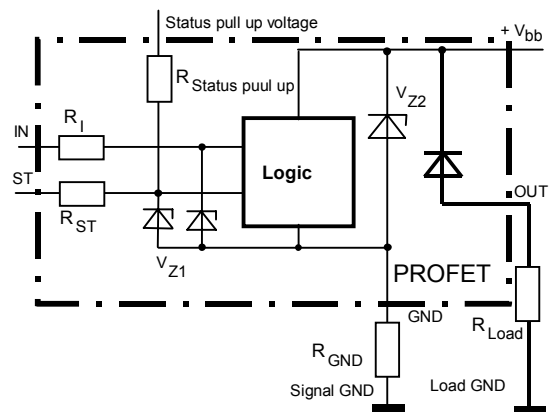


Inductive and overvoltage output clamp, OUT1 or OUT2



V_{ON} clamped to $V_{ON(CL)} = 64\ V$ typ.

Overvolt. and reverse batt. protection



$V_{Z1} = 6.1\ V$ typ., $V_{Z2} = 63\ V$ typ., $R_{GND} = 150\ \Omega$,
 $R_I = 850\ \Omega$ typ., $R_{ST} = 20\ k\Omega$ typ., $R_{pull\ up} = 12\ k\Omega$ typ
 In case of reverse battery the load current has to be limited by the load. Temperature protection is not active

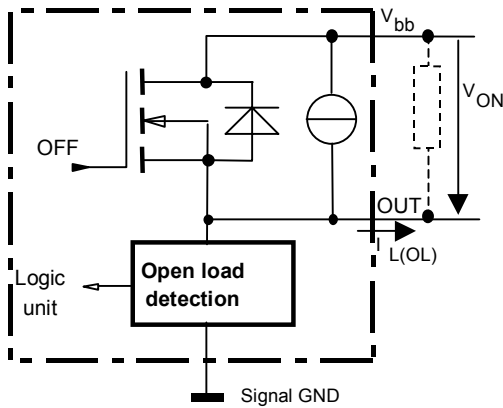
Open-load detection, OUT1 or OUT2

OFF-state diagnostic condition:

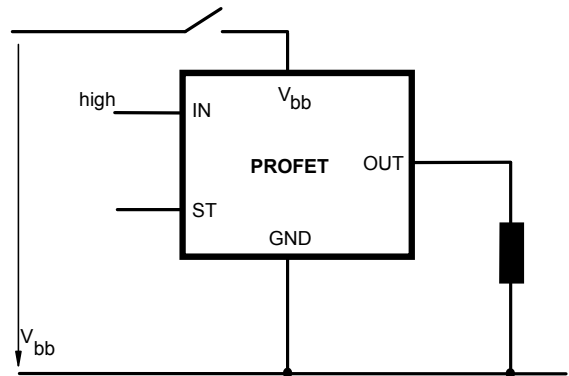
Open load, if $V_{OUT} > 2.7\text{ V typ. (IN low)}$

$I_{L(OL)}$ typ. $2\mu\text{A}$

An external resistor can be used to increase the open load detection current



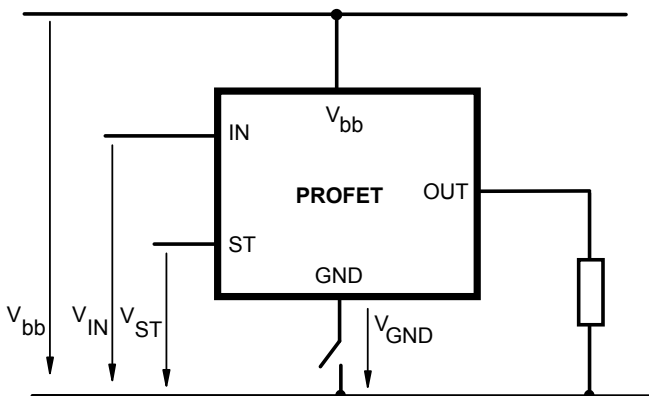
V_{bb} disconnect with energized inductive load



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 12) each switch is protected against loss of V_{bb} .

Consider at your PCB layout that in the case of V_{bb} disconnection with energized inductive load all the load current flows through the GND connection.

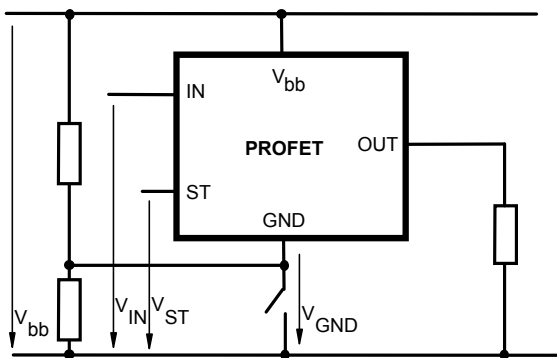
GND disconnect



Any kind of load.

Due to $V_{GND} > 0$, no $V_{ST} = \text{low signal}$ available.

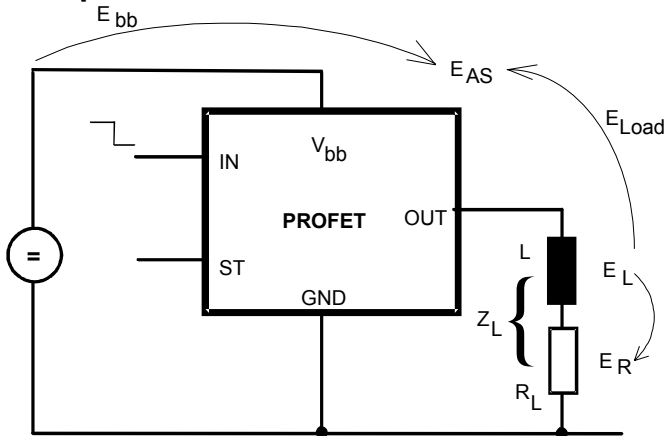
GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off

Due to $V_{GND} > 0$, no $V_{ST} = \text{low signal}$ available.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = 1/2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

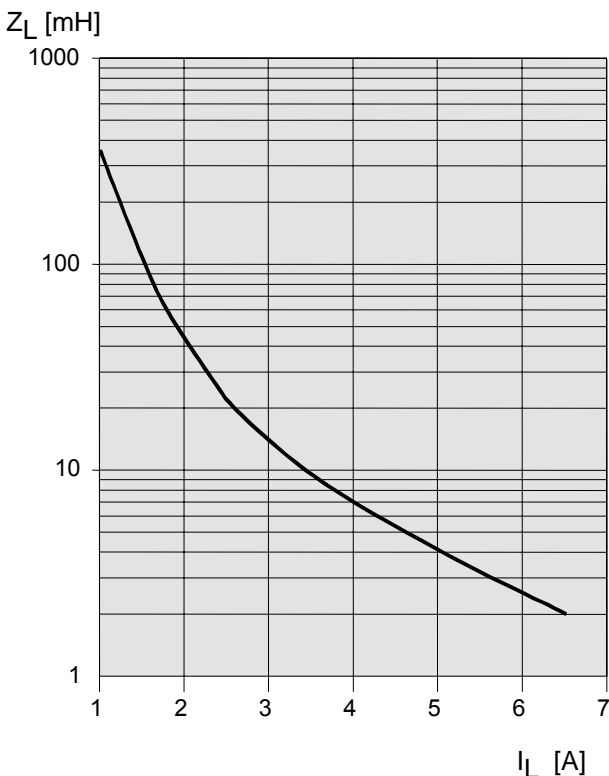
$$E_{AS} = E_{bb} + E_L - E_R = \int V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for $R_L > 0 \Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

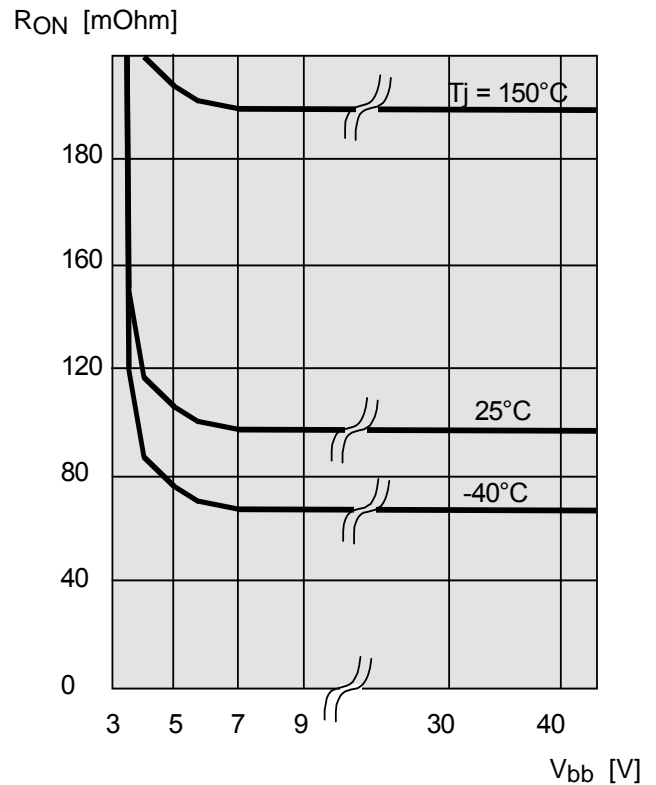
Maximum allowable load inductance for a single switch off (one channel)⁵⁾

$L = f(I_L); T_{j,start} = 150^\circ C, V_{bb} = 12 V, R_L = 0 \Omega$



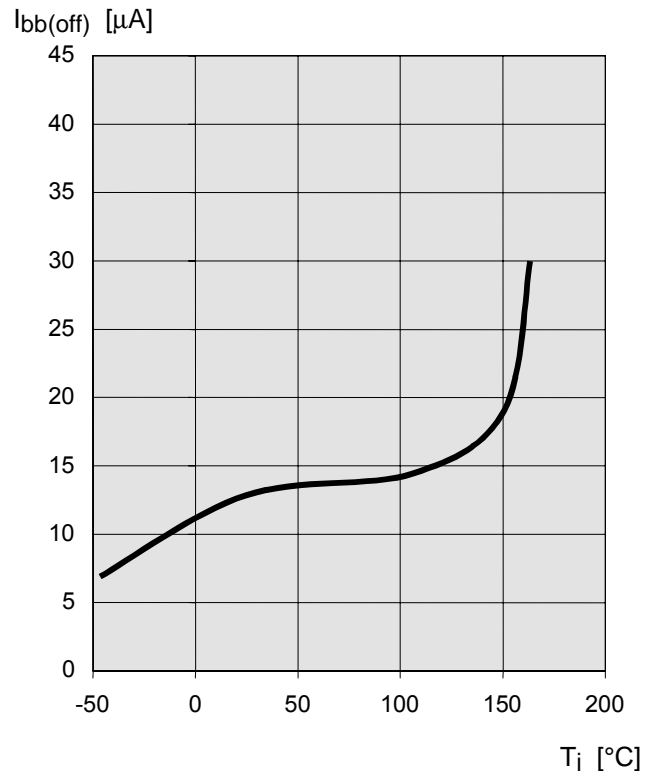
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j); I_L = 2 A, I_N = \text{high}$



Typ. standby current

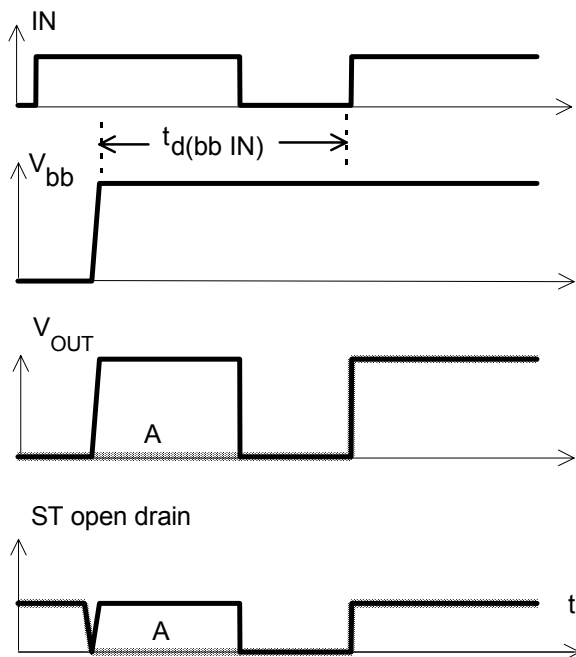
$I_{bb(off)} = f(T_j); V_{bb} = 9...34 V, I_{N1,2,3,4} = \text{low}$



Timing diagrams

All channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: V_{bb} turn on, :



in case of too early V_{IN} =high the device may not turn on (curve A)
 $t_{d(bb IN)}$ approx. 150 μ s

Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

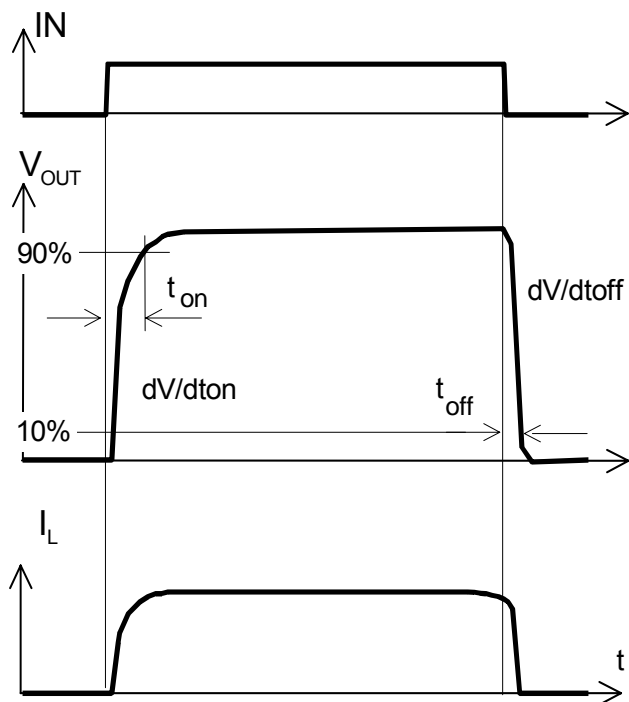


Figure 2b: Switching an inductive load

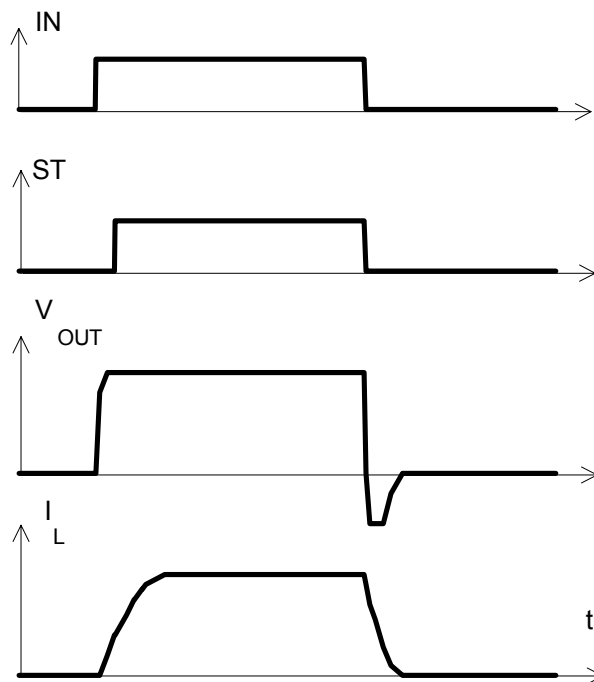
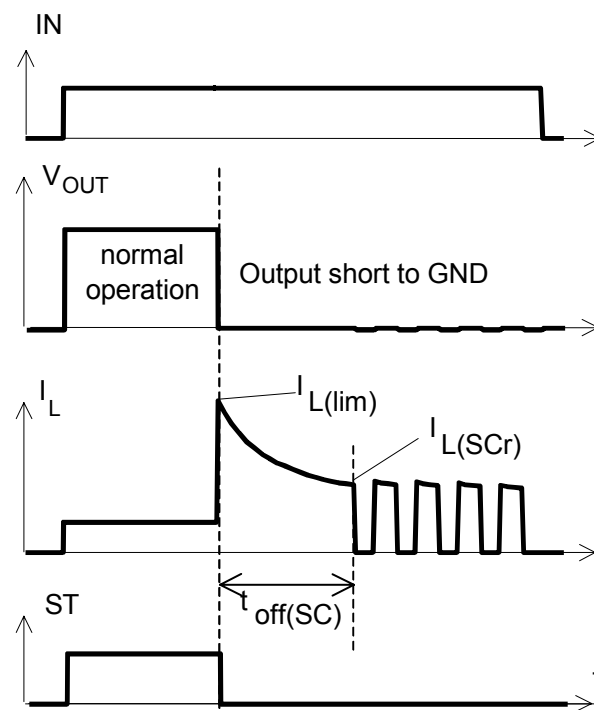


Figure 3a: Short circuit: shut down by overtemperature, reset by cooling



Heating up requires several milliseconds, depending on external conditions. External shutdown in response to status fault signal recommended.

Figure 4a: Overtemperature:
Reset if $T_j < T_{jt}$

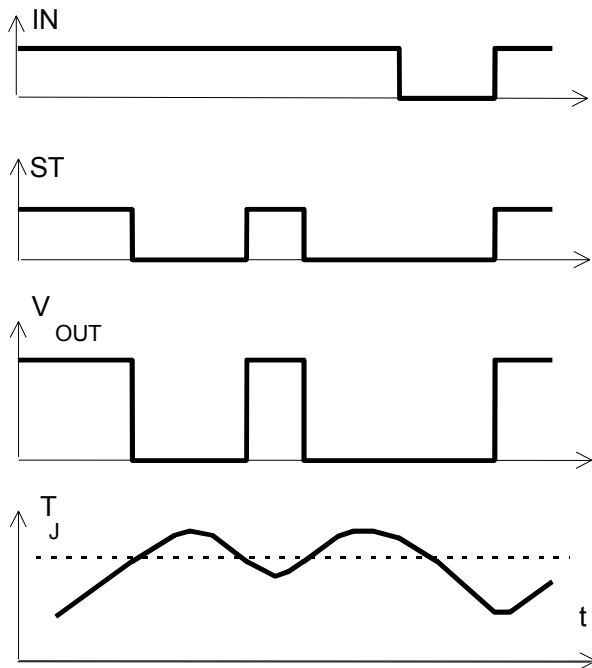
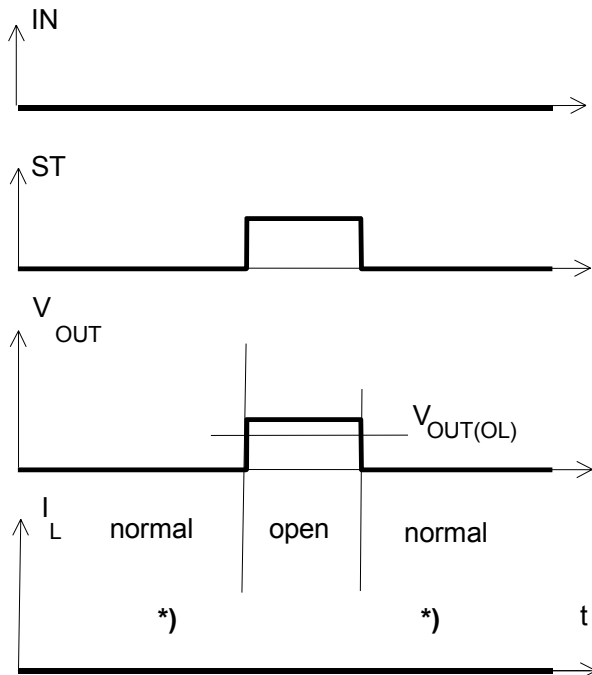
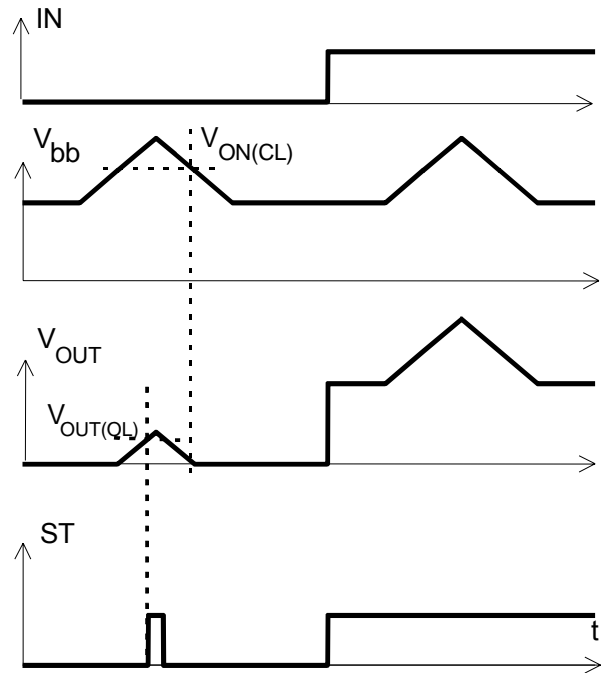


Figure 5a: Open load, : detection in OFF-state, open load occurs in off-state



*) $I_L = 2 \mu A$ typ. $V_{OUT} > 2.7V$

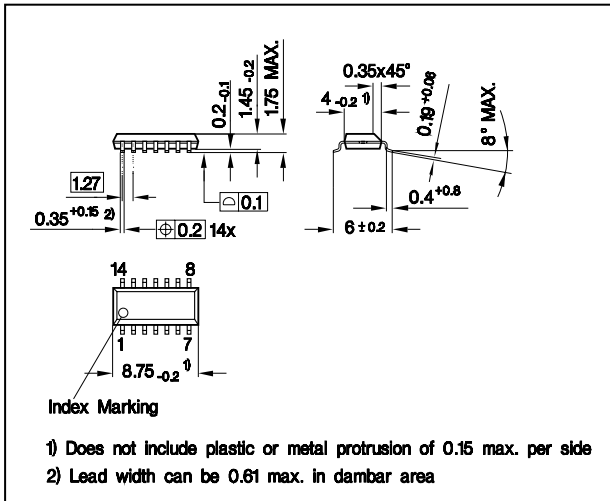
Figure 6: Overvoltage, no shutdown:



Package and Ordering Code

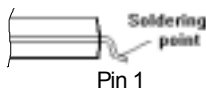
Standard: P-DSO-14-9

Sales Code	BTS 723 GW
Ordering Code	Q67060-S7501

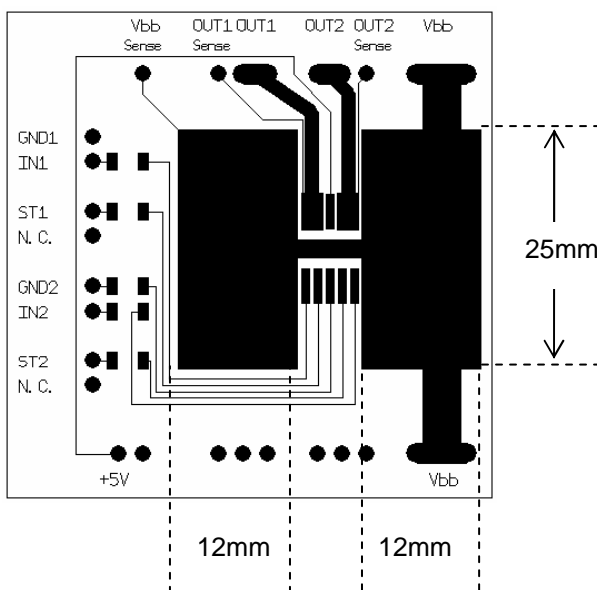


All dimensions in millimetres

Definition of soldering point with temperature T_s :
 upper side of solder edge of device pin 1.



Printed circuit board (FR4, 1.5mm thick, one layer 70 μ m, 6cm² active heatsink area) as a reference for max. power dissipation P_{tot} , nominal load current $I_{L(NOM)}$ and thermal resistance R_{thja}



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