High-Efficiency Low-Side N-Channel Controller for Switching Regulator

Check for Samples: LM3478, LM3478-Q1

FEATURES

- **LM3478Q in VSSOP-8 package is AEC-Q100 qualified and manufactured on an Automotive Grade Flow**
- **8-lead VSSOP-8 and SOIC-8 packages**
- **Internal push-pull driver with 1A peak current capability**
- **Current limit and thermal shutdown**
- **Frequency compensation optimized with a capacitor and a resistor**
- **Internal soft start**
- **Current Mode Operation**
- **Undervoltage Lockout with hysteresis**

APPLICATIONS

- **Distributed Power Systems**
- **Battery Chargers**
- **Offline Power Supplies**
- **Telecom Power Supplies**
- **Automotive Power Systems**

KEY SPECIFICATIONS

- **Wide supply voltage range of 2.97V to 40V**
- **100kHz to 1MHz Adjustable clock frequency**
- **±2.5% (over temperature) internal reference**
- **10µA shutdown current (over temperature)**

DESCRIPTION

The LM3478 is a versatile Low-Side N-Channel MOSFET controller for switching regulators. It is suitable for use in topologies requiring a low side MOSFET, such as boost, flyback, SEPIC, etc. Moreover, the LM3478 can be operated at extremely high switching frequency in order to reduce the overall solution size. The switching frequency of the LM3478 can be adjusted to any value between 100kHz and 1MHz by using a single external resistor. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.

The LM3478 has built in features such as thermal shutdown, short-circuit protection, over voltage protection, etc. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Typical Application Circuit

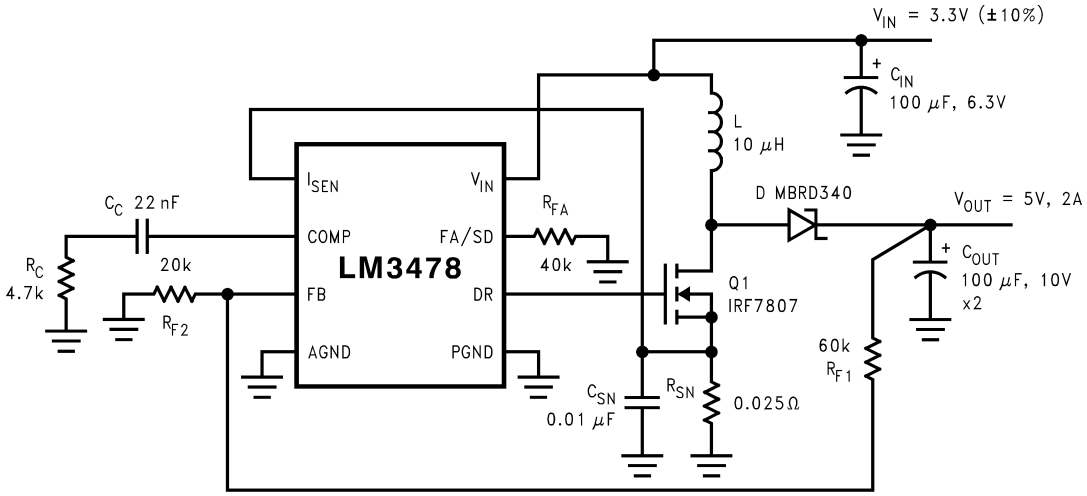


Figure 1. Typical High Efficiency Step-Up (Boost) Converter

Connection Diagram

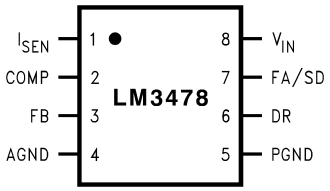


Figure 2. 8-Lead VSSOP-8 Package

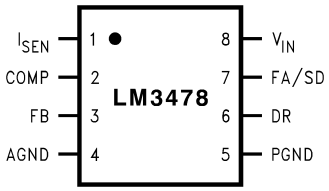


Figure 3. 8-Lead SOIC-8 Package

Table 1. Pin Descriptions

Pin Name	Pin No.	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP	2	Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop.
FB	3	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26V at this pin.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	Drive pin. The gate of the external MOSFET should be connected to this pin.
FA/SD	7	Frequency adjust and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. A high level on this pin for longer than 30 µs will turn the device off. The device will then draw less than 10µA from the supply.
V_{IN}	8	Power Supply Input pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Input Voltage		45V
FB Pin Voltage		-0.4V < V_{FB} < 7V
FA/SD Pin Voltage		-0.4V < $V_{FA/SD}$ < 7V
Peak Driver Output Current (<10µs)		1.0A
Power Dissipation		Internally Limited
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+150°C
ESD Susceptibility Human Body Model (2)		2kV
Lead Temperature	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	260°C
DR Pin Voltage		−0.4V ≤ VDR ≤ 8V
I_{SEN} Pin Voltage		500mV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.
(2) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Ratings (1)

Supply Voltage	2.97V ≤ V_{IN} ≤ 40V
Junction Temperature Range	−40°C ≤ T_J ≤ +125°C
Switching Frequency	100kHz ≤ F_{SW} ≤ 1MHz

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V, R_{FA} = 40kΩ

Symbol	Parameter	Conditions	Typical	Limit	Unit
V_{FB}	Feedback Voltage	V_{COMP} = 1.4V, 2.97 ≤ V_{IN} ≤ 40V	1.26	 1.2416/**1.228** 1.2843/**1.292**	V V(min) V(max)
ΔV_{LINE}	Feedback Voltage Line Regulation	2.97 ≤ V_{IN} ≤ 40V	0.001		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{EAO} Source/Sink	±0.5		%/A (max)
V_{UVLO}	Input Undervoltage Lock-out		2.85	 **2.97**	V V(max)
$V_{UV(HYS)}$	Input Undervoltage Lock-out Hysteresis		170	 **130** **210**	mV mV (min) mV (max)
F_{nom}	Nominal Switching Frequency	R_{FA} = 40KΩ	400	 **350** **440**	kHz kHz(min) kHz(max)
$R_{DS1\ (ON)}$	Driver Switch On Resistance (top)	I_{DR} = 0.2A, V_{IN}= 5V	16		Ω
$R_{DS2\ (ON)}$	Driver Switch On Resistance (bottom)	I_{DR} = 0.2A	4.5		Ω
$V_{DR\ (max)}$	Maximum Drive Voltage Swing(1)	V_{IN} < 7.2V	V_{IN}		V
		V_{IN} ≥ 7.2V	7.2		
D_{max}	Maximum Duty Cycle(2)		100		%
T_{min} (on)	Minimum On Time		325	 **210** **600**	nsec nsec(min) nsec(max)
I_{SUPPLY}	Supply Current (non-switching)	(3)	2.7	 **3.3**	mA mA (max)
I_Q	Quiescent Current in Shutdown Mode	$V_{FA/SD}$ = 5V (4), V_{IN} = 5V	5	 **10**	µA µA (max)
V_{SENSE}	Current Sense Threshold Voltage	V_{IN} = 5V	156	 135/ **125** 180/ **190**	mV mV (min) mV (max)
V_{SC}	Short-Circuit Current Limit Sense Voltage	V_{IN} = 5V	343	**250** **415**	mV mV (min) mV (max)
V_{SL}	Internal Compensation Ramp Voltage	V_{IN} = 5V	92	 **52** **132**	mV mV(min) mV(max)
V_{SL} ratio	V_{SL}/V_{SENSE}		0.49	0.30 0.70	(min) (max)
V_{OVP}	Output Over-voltage Protection (with respect to feedback voltage) (5)	V_{COMP} = 1.4V	50	 32/ **25**	mV mV(min)
		VSSOP Package		78/ **85**	mV(max)
		SOIC Package		78/**100**	mV(max)
$V_{OVP(HYS)}$	Output Over-Voltage Protection Hysteresis(5)	V_{COMP} = 1.4V	60	 **20** **110**	mV mV(min) mV(max)

(1) The voltage on the drive pin, V_{DR} is equal to the input voltage when input voltage is less than 7.2V. V_{DR} is equal to 7.2V when the input voltage is greater than or equal to 7.2V.
(2) The limits for the maximum duty cycle can not be specified since the part does not permit less than 100% maximum duty cycle operation.
(3) For this test, the FA/SD pin is pulled to ground using a 40K resistor.
(4) For this test, the FA/SD pin is pulled to 5V using a 40K resistor.
(5) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The overvoltage protection threshold is given by adding the feedback voltage, V_{FB} to the over-voltage protection specification.

Electrical Characteristics (continued)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range**. Unless otherwise specified, V_{IN} = 12V, R_{FA} = 40kΩ

Symbol	Parameter	Conditions	Typical	Limit	Unit
Gm	Error Amplifier Transconductance	V_{COMP} = 1.4V I_{EAO} = 100µA (Source/Sink)	800	600/ **365** 1000/ **1265**	µmho µmho (min) µmho (max)
A_{VOL}	Error Amplifier Voltage Gain	V_{COMP} = 1.4V I_{EAO} = 100µA (Source/Sink)	38	**26** **44**	V/V V/V (min) V/V (max)
I_{EAO}	Error Amplifier Output Current (Source/ Sink)	Source, V_{COMP} = 1.4V, V_{FB} = 0V	110	80/ **50** 140/ **180**	µA µA (min) µA (max)
		Sink, V_{COMP} = 1.4V, V_{FB} = 1.4V	−140	−100/ **−85** −180/ **−185**	µA µA (min) µA (max)
V_{EAO}	Error Amplifier Output Voltage Swing	Upper Limit V_{FB} = 0V COMP Pin = Floating	2.2	**1.8** **2.4**	V V(min) V(max)
		Lower Limit V_{FB} = 1.4V	0.56	**0.2** **1.0**	V V(min) V(max)
T_{SS}	Internal Soft-Start Delay	V_{FB} = 1.2V, V_{COMP} = Floating	4		msec
T_r	Drive Pin Rise Time	Cgs = 3000pf, V_{DR} = 0 to 3V	25		ns
T_f	Drive Pin Fall Time	Cgs = 3000pf, V_{DR} = 0 to 3V	25		ns
V_{SD}	Shutdown threshold (6)	Output = High	1.27	**1.4**	V V (max)
		Output = Low	0.65	**0.3**	V V (min)
I_{SD}	Shutdown Pin Current	V_{SD} = 5V	−1		µA
		V_{SD} = 0V	+1		
I_{FB}	Feedback Pin Current		15		nA
T_{SD}	Thermal Shutdown		165		°C
T_{sh}	Thermal Shutdown Hysteresis		10		°C
θ_{JA}	Thermal Resistance	VSSOP Package	200		°C/W
		SOIC Package	151		

(6) The FA/SD pin should be pulled to V_{IN} through a resistor to turn the regulator off. The voltage on the FA/SD pin must be above the maximum limit for Output = High to keep the regulator off and must be below the limit for Output = Low to keep the regulator on.

Typical Performance Characteristics

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

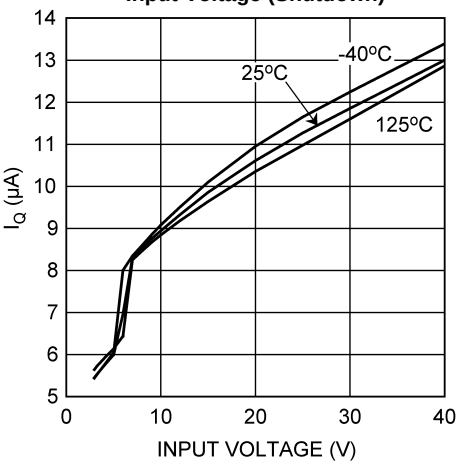


Figure 4.

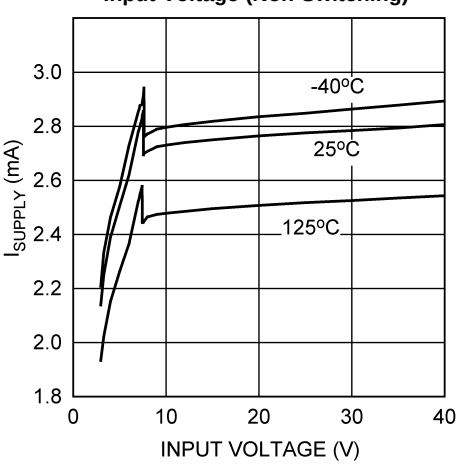


Figure 5.

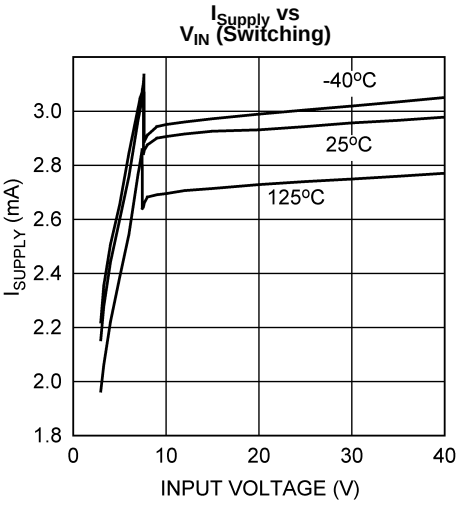


Figure 6.

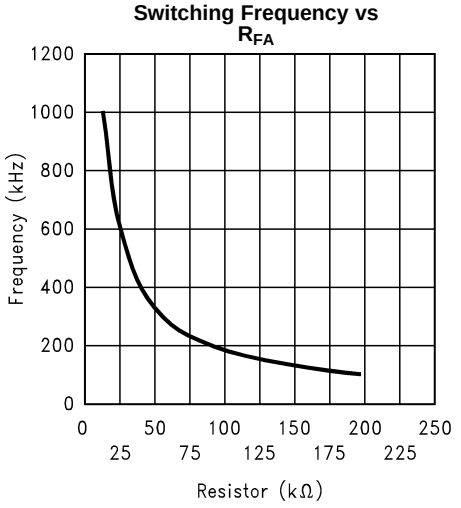


Figure 7.

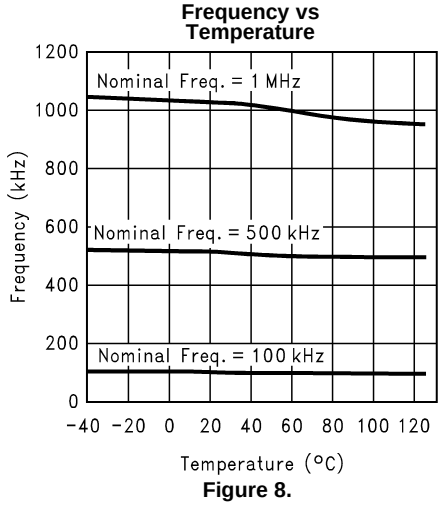


Figure 8.

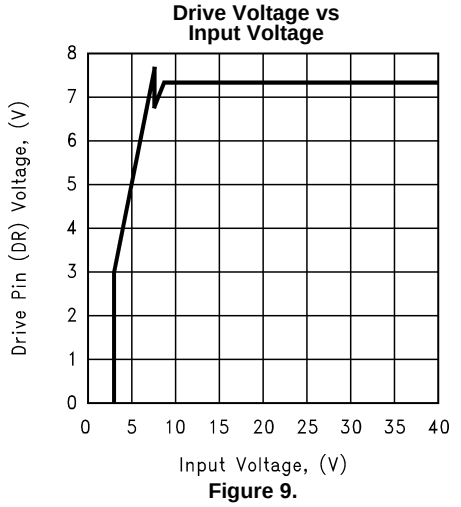


Figure 9.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

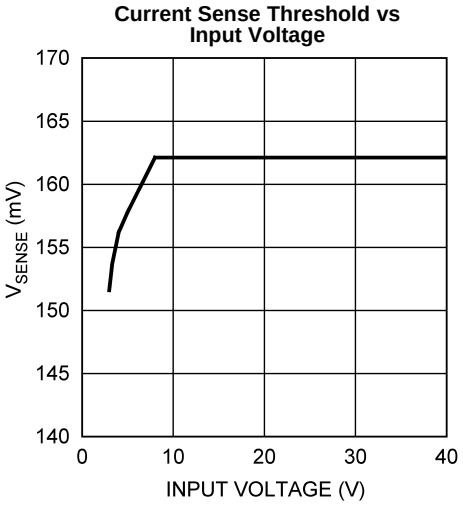


Figure 10.

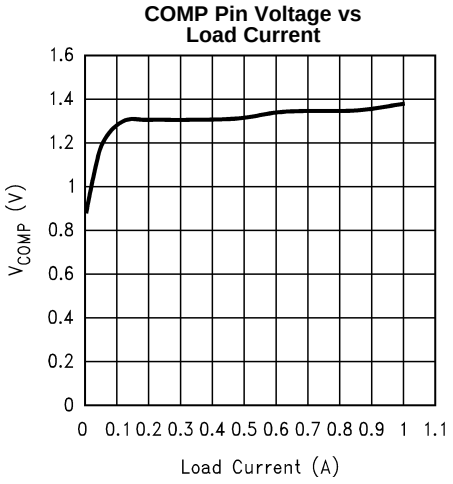


Figure 11.

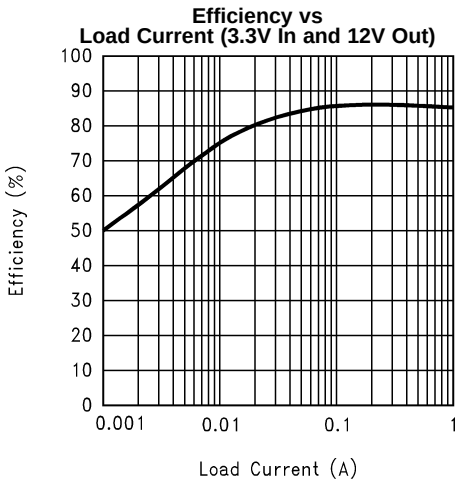


Figure 12.

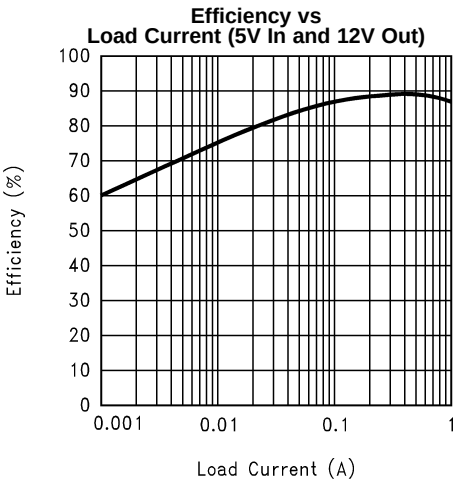


Figure 13.

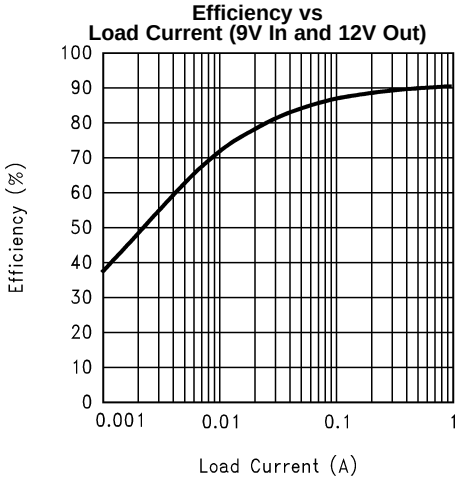


Figure 14.

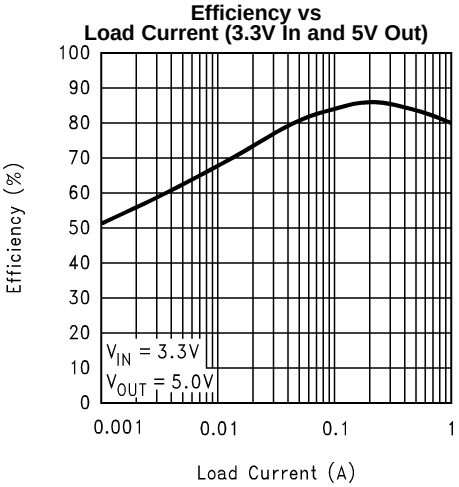


Figure 15.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

Error Amplifier Gain

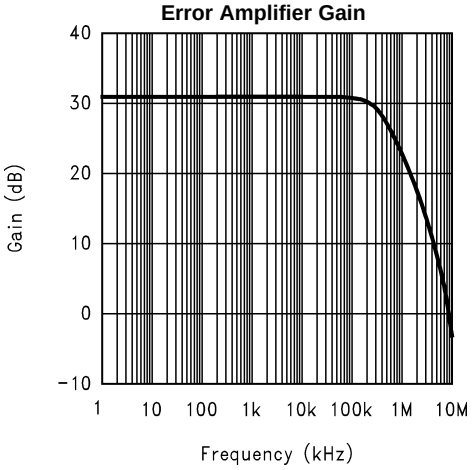


Figure 16.

Error Amplifier Phase

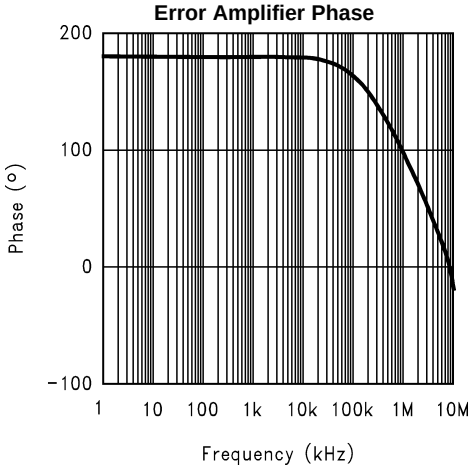


Figure 17.

COMP Pin Source Current vs Temperature

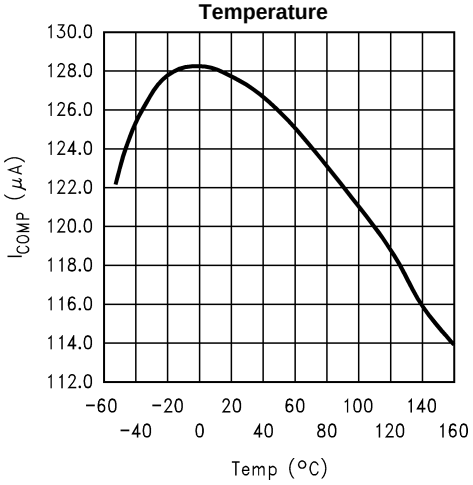


Figure 18.

Short Circuit Sense Voltage vs Input Voltage

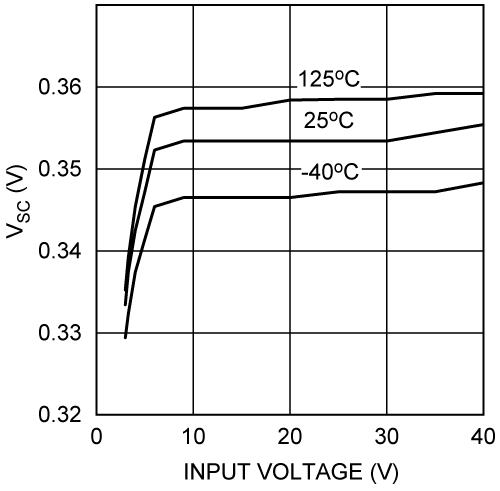


Figure 19.

Compensation Ramp vs Compensation Resistor

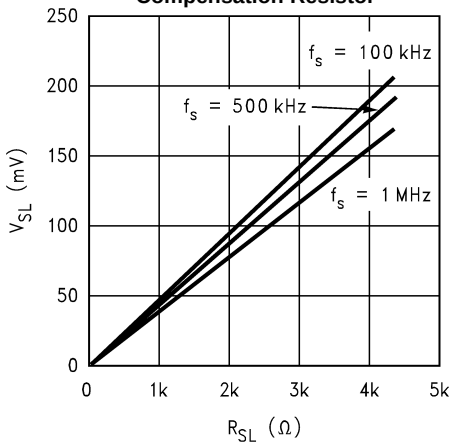


Figure 20.

Shutdown Threshold Hysteresis vs Temperature

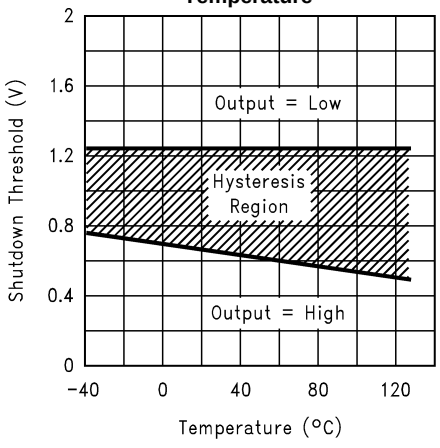


Figure 21.

Typical Performance Characteristics (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C.

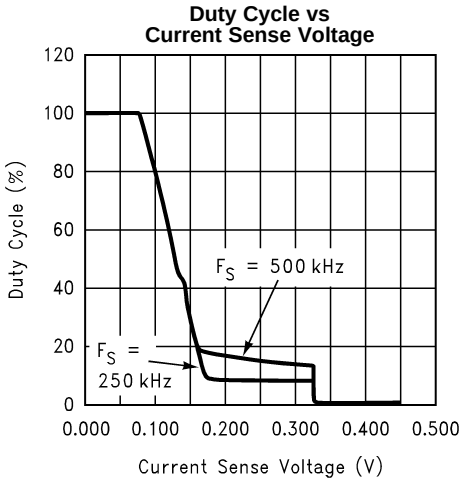


Figure 22.

FUNCTIONAL BLOCK DIAGRAM

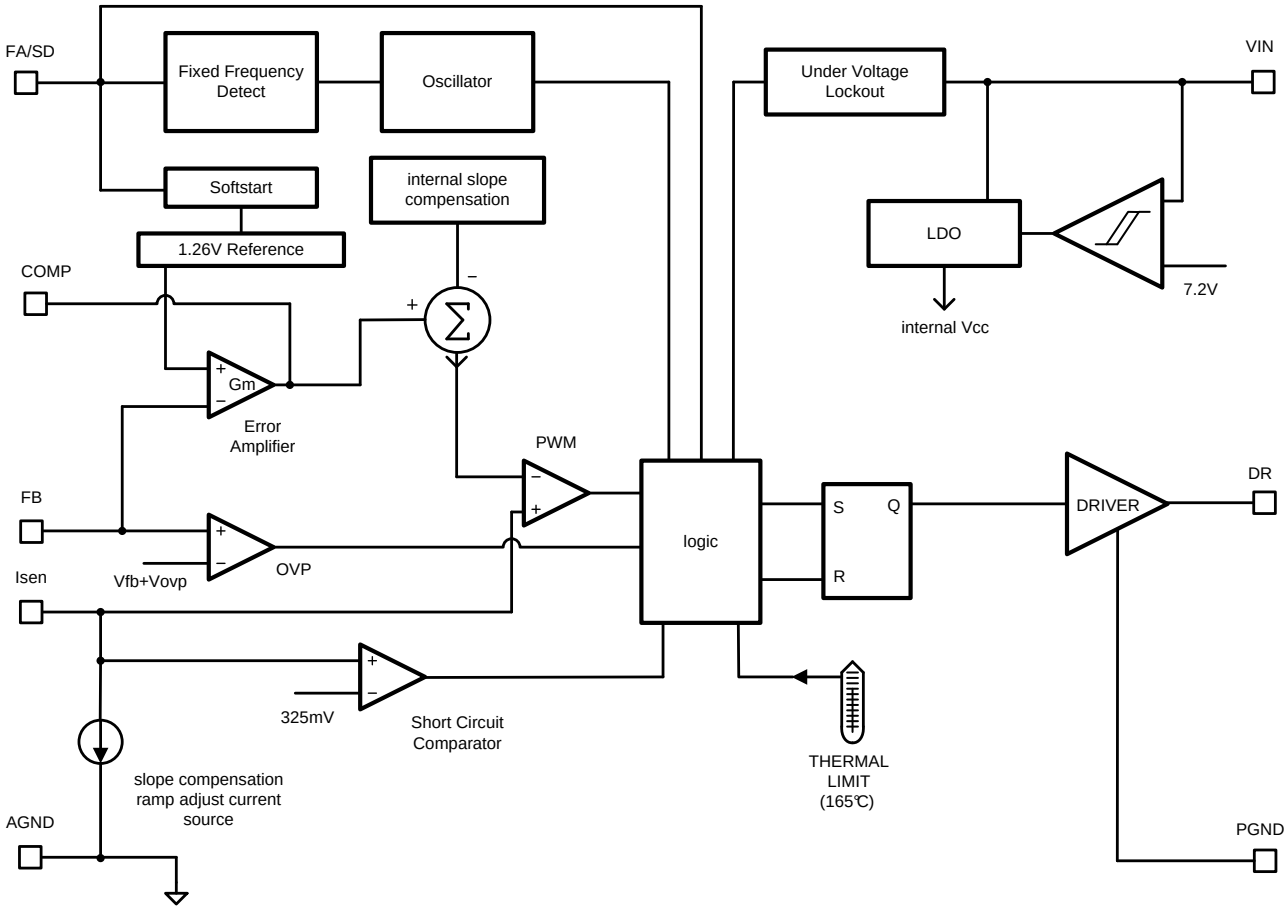


Figure 23.

FUNCTIONAL DESCRIPTION

The LM3478 uses a fixed frequency, Pulse Width Modulated (PWM) current mode control architecture. The block diagram above shows the basic functionality. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in Figure 25. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is about 325ns and is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET in on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the LM3478 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

OVER VOLTAGE PROTECTION

The LM3478 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (pin 3). If at anytime the voltage at the feedback pin rises to V_{FB}+ V_{OVP}, OVP is triggered. See ELECTRICAL CHARACTERISTICS section for limits on V_{FB} and V_{OVP}.

OVP will cause the drive pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3478 will begin switching again when the feedback voltage reaches V_{FB} + (V_{OVP} - $V_{OVP(HYS)}$). See ELECTRICAL CHARACTERISTICS for limits on $V_{OVP(HYS)}$.

OVP can be triggered if the unregulated input voltage crosses 7.2V, the output voltage will react as shown in Figure 24. The internal bias of the LM3478 comes from either the internal LDO as shown in the block diagram or the voltage at the Vin pin is used directly. At Vin voltages lower than 7.2V the internal IC bias is the Vin voltage and at voltages above 7.2V the internal LDO of the LM3478 provides the bias. At the switch over threshold at 7.2V a sudden small change in bias voltage is seen by all the internal blocks of the LM3478. The control voltage shifts because of the bias change, the PWM comparator tries to keep regulation. To the PWM comparator, the scenario is identical to a step change in the load current, so the response at the output voltage is the same as would be observed in a step load change. Hence, the output voltage overshoot here can also trigger OVP. The LM3478 will regulate in hysteretic mode for several cycles, or may not recover and simply stay in hysteretic mode until the load current drops or Vin is not crossing the 7.2V threshold anymore. Note that the output is still regulated in hysteretic mode.

Depending on the requirements of the application there is some influence one has over this effect. The threshold of 7.2V can be shifted to higher voltages by adding a resistor in series with Vin. In case Vin is right at the threshold of 7.2V it can happen that the threshold is crossed over and over due to some slight ripple on Vin. To minimize the effect on the output voltage one can filter the Vin pin with an RC filter.

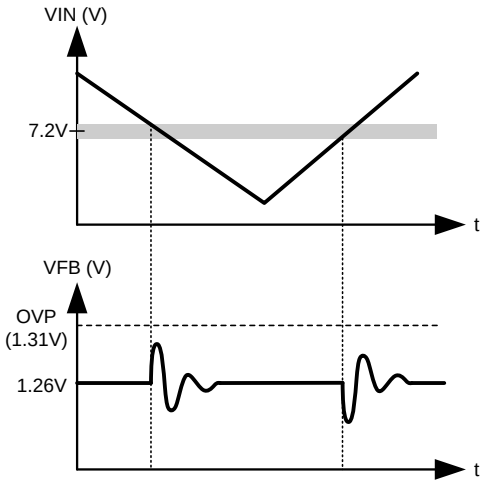


Figure 24. The Feedback Voltage Experiences an Oscillation if the Input Voltage crosses the 7.2V Internal Bias Threshold

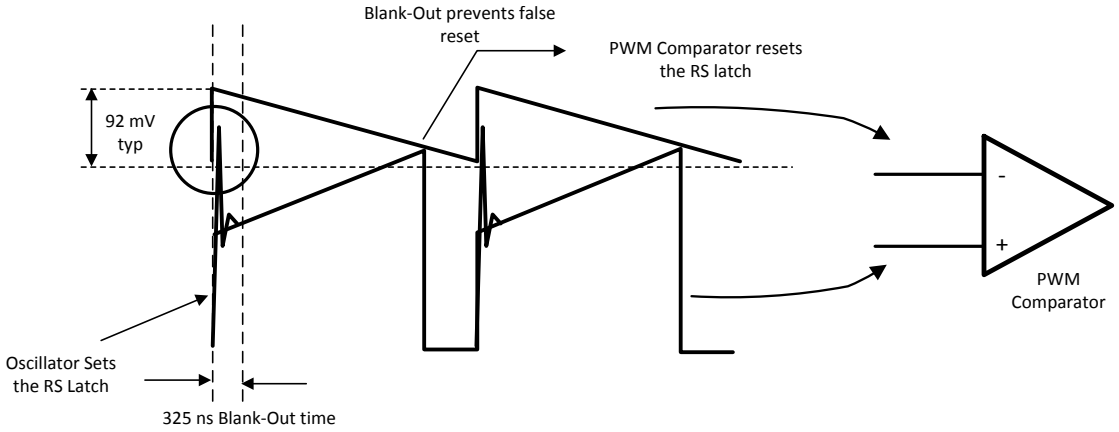


Figure 25. Basic Operation of the PWM Comparator

SLOPE COMPENSATION RAMP

The LM3478 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is also easy to parallel power stages using current mode control since current sharing is automatic. However, current mode control has an inherent instability for duty cycles greater than 50%, as shown in Figure 26.

A small increase in the load current causes the switch current to increase by ΔI_0. The effect of this load change is ΔI_1.

The two solid waveforms shown are the waveforms compared at the internal pulse width modulator, used to generate the MOSFET drive signal. The top waveform with the slope S_e is the internally generated control waveform V_C. The bottom waveform with slopes S_n and S_f is the sensed inductor current waveform V_{SEN}.

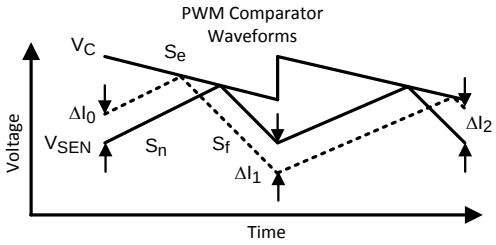


Figure 26. Sub-Harmonic Oscillation for D>0.5 and Compensation Ramp to Avoid Sub-Harmonic Oscillation

Sub-harmonic Oscillation can be easily understood as a geometric problem. If the control signal does not have slope, the slope representing the inductor current ramps up until the control signal is reached and then slopes down again. If the duty cycle is above 50%, any perturbation will not converge but diverge from cycle to cycle and causes sub-harmonic oscillation.

It is apparent that the difference in the inductor current from one cycle to the next is a function of S_n, S_f and S_e as follows:

$$\Delta I_n = \frac{S_f - S_e}{S_n + S_e} \Delta I_{n-1} \quad (1)$$

Hence, if the quantity $(S_f - S_e)/(S_n + S_e)$ is greater than 1, the inductor current diverges and subharmonic oscillation results. This counts for all current mode topologies. The LM3478 has some internal slope compensation V_{SL} which is enough for many applications above 50% duty cycle to avoid subharmonic oscillation .

For boost applications, the slopes S_e, S_f and S_n can be calculated with the formulas below:

$$S_e = V_{SL} \times f_s \quad (2)$$

$$S_f = R_{sen} \times (V_{OUT} - V_{IN})/L \quad (3)$$

$$S_n = V_{IN} \times R_{sen}/L \quad (4)$$

When S_e increases then the factor which determines if subharmonic oscillation will occur decreases. When the duty cycle is greater than 50%, and the inductance becomes less, the factor increases.

For more flexibility slope compensation can be increased by adding one external resistor, R_{SL}, in the Isens path. Figure 27 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the LM3478. When using external slope compensation, the formula for S_e becomes:

$$S_e = (V_{SL} + (K \times R_{SL})) \times f_s \quad (5)$$

A typical value for factor K is 40 µA.

The factor changes with switching frequency. Figure 28 is used to determine the factor K for individual applications and the formula below gives the factor K.

$$K = \Delta V_{SL} / R_{SL} \quad (6)$$

It is a good design practice to only add as much slope compensation as needed to avoid subharmonic oscillation. Additional slope compensation minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current.

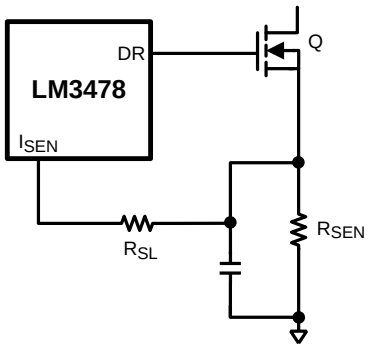


Figure 27. Adding External Slope Compensation

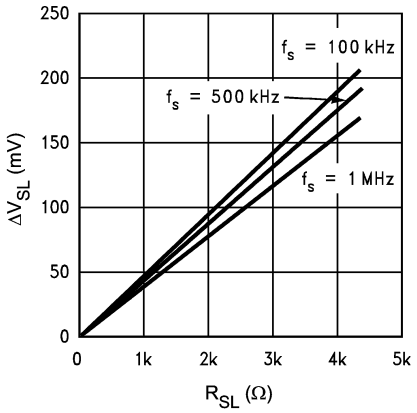


Figure 28. External Slope Compensation ΔV_{SL} vs R_{SL}

FREQUENCY ADJUST/SHUTDOWN

The switching frequency of the LM3478 can be adjusted between 100kHz and 1MHz using a single external resistor. This resistor must be connected between FA/SD pin and ground, as shown in Figure 29. To determine the value of the resistor required for a desired switching frequency refer to Typical Performance Characteristics or use the following equation:

$$R_{FA} = 4.503 \times 10^{11} \times f_S^{-1.26} \quad (7)$$

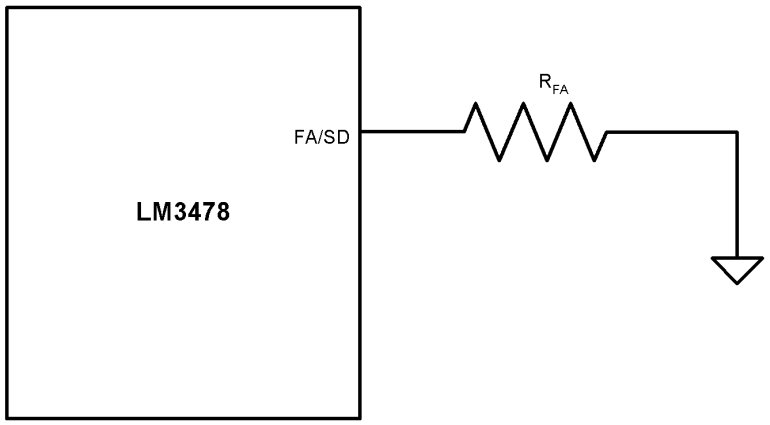


Figure 29. Frequency Adjust

The FA/SD pin also functions as a shutdown pin. If a high signal (>1.35V) appears on the FA/SD pin, the LM3478 stops switching and goes into a low current mode. The total supply current of the IC reduces to less than 10 µA under these conditions. Figure 30 shows implementation of the shutdown function when operating in frequency adjust mode. In this mode a high signal for more than 30us shuts down the IC. However, the voltage on the FA/SD pin should be always less than the absolute maximum of 7V to avoid any damage to the device.

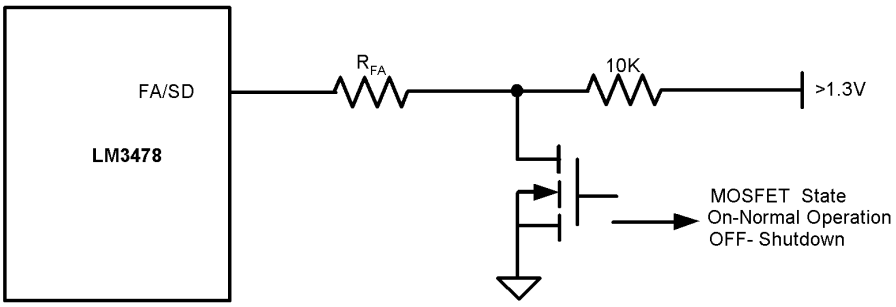


Figure 30. Shutdown Operation in Frequency Adjust Mode

SHORT-CIRCUIT PROTECTION

When the voltage across the sense resistor measured on the I_{SEN} pin exceeds 343 mV, short circuit current limit protection gets activated. A comparator inside the LM3478 reduces the switching frequency by a factor of 5 and maintains this condition until the short is removed. In normal operation the sensed current will trigger the power MOSFET to turn off. During the blanking interval the PWM comparator will not react to an over current so that this additional 343 mV current limit threshold is implemented to protect the device in a short circuit or severe overload condition.

Typical Applications

The LM3478 may be operated in either the continuous (CCM) or the discontinuous current conduction mode (DCM). The following applications are designed for the CCM operation. This mode of operation has higher efficiency and usually lower EMI characteristics than the DCM.

BOOST CONVERTER

The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost converter is shown in Figure 31. In the CCM (when the inductor current never reaches zero at steady state), the boost regulator operates in two states. In the first state of operation, MOSFET Q is turned on and energy is stored in the inductor. During this state, diode D is reverse biased and load current is supplied by the output capacitor, Cout.

In the second state, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and the output capacitor. The ratio of the switch on time to the total period is the duty cycle D:

$$D = 1 - (V_{in} / V_{out}) \quad (8)$$

Including the voltage drop across the MOSFET and the diode the definition for the duty cycle is:

$$D = 1 - ((V_{in} - V_q)/(V_{out} + V_d)) \quad (9)$$

V_d is the forward voltage drop of the diode and V_q is the voltage drop across the MOSFET when it is on.

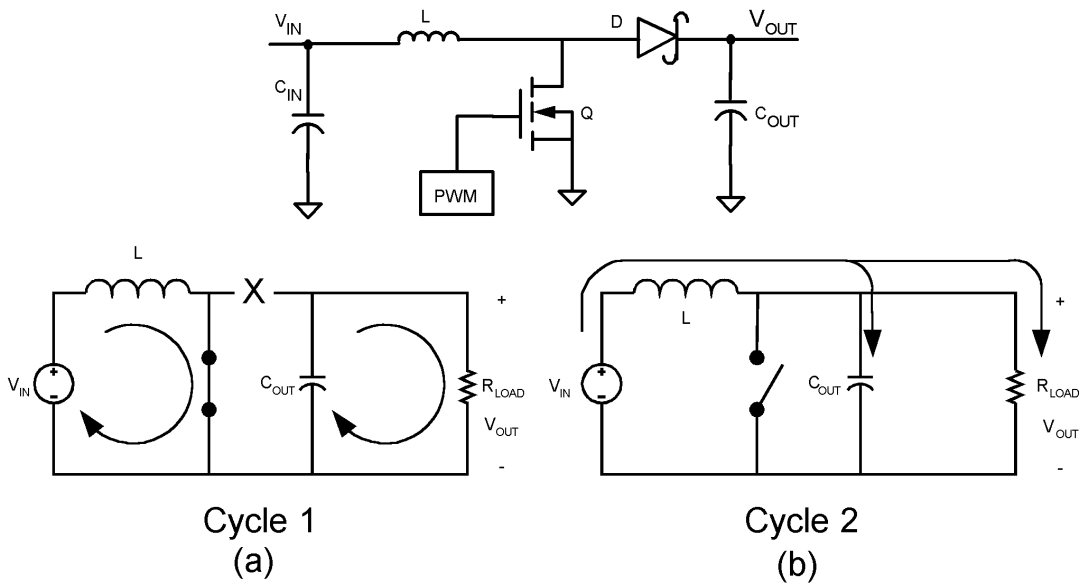


Figure 31. Simplified Boost Converter
(a) First Cycle Operation
(b) Second Cycle of Operation

POWER INDUCTOR SELECTION

The inductor is one of the two energy storage elements in a boost converter. Figure 32 shows how the inductor current varies during a switching cycle. The current through an inductor is quantified by the following relationship of L, I_L and V_L:

$$V_L(t) = L \frac{di_L(t)}{dt} \tag{10}$$

The important quantities in determining a proper inductance value are I_L (the average inductor current) and ΔI_L (the inductor current ripple). If ΔI_L is larger than I_L, the inductor current will drop to zero for a portion of the cycle and the converter will operate in the DCM. All the analysis in this datasheet assumes operation in the CCM. To operate in the CCM, the following condition must be met:

$$L > \frac{D(1-D)V_{IN}}{2I_{OUT}f_S} \tag{11}$$

Choose the minimum Iout to determine the minimum inductance value. A common choice is to set ΔI_L to 30% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter the peak inductor current is:

$$I_{LPEAK} = \text{Average } I_{L(max)} + \Delta I_{L(max)} \tag{12}$$

$$\text{Average } I_{L(max)} = I_{out} / (1-D) \tag{13}$$

$$\Delta I_{L(max)} = D \times V_{in} / (2 \times f_s \times L) \tag{14}$$

An inductor size with ratings higher than these values has to be selected. If the inductor is not properly rated, saturation will occur and may cause the circuit to malfunction.

The LM3478 can be set to switch at very high frequencies. When the switching frequency is high, the converter can be operated with very small inductor values. The LM3478 senses the peak current through the switch which is the same as the peak inductor current as calculated above.

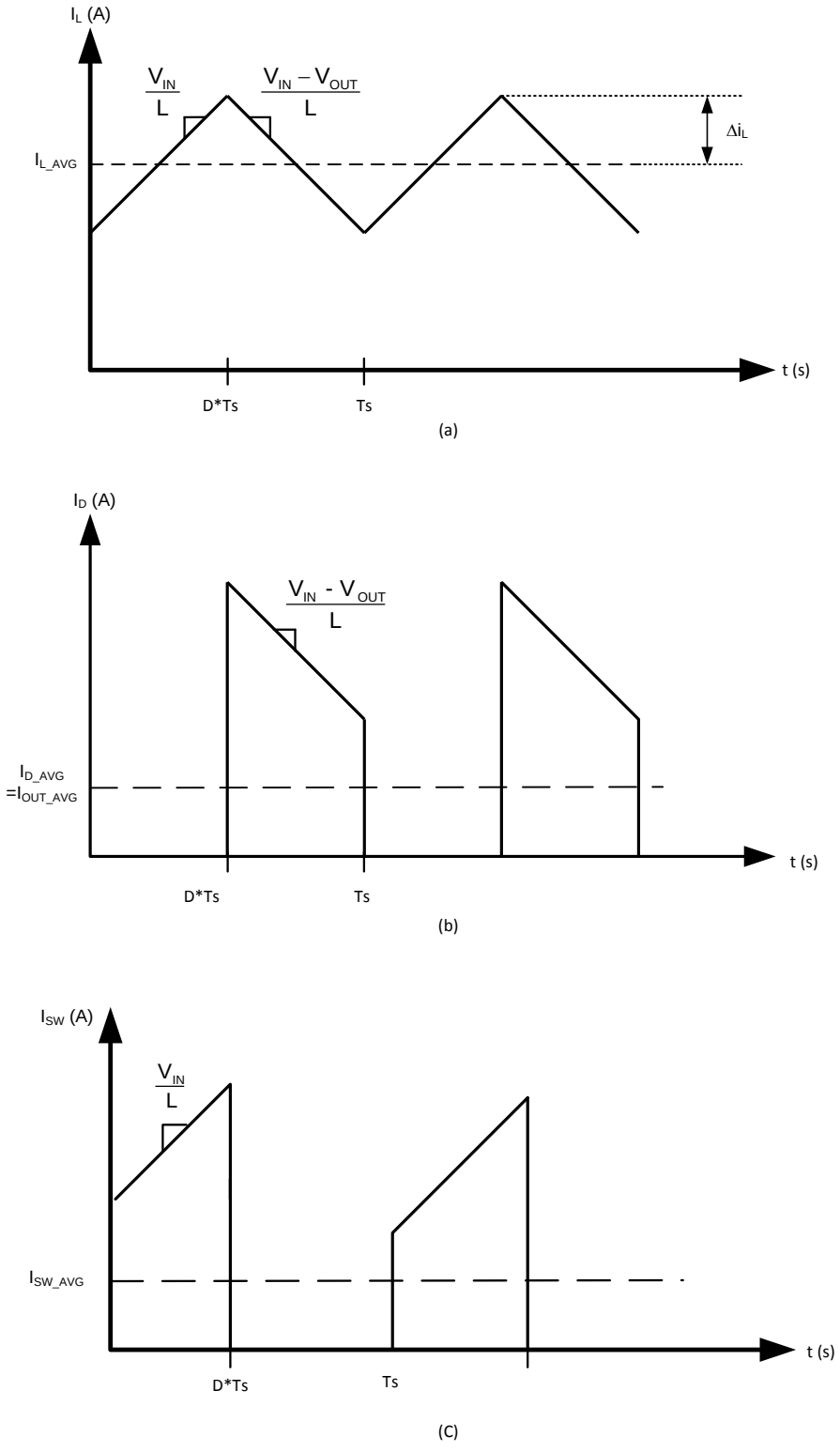


Figure 32. Inductor Current and Diode Current

PROGRAMMING THE OUTPUT VOLTAGE

The output voltage can be programmed using a resistor divider between the output and the FB pin. The resistors are selected such that the voltage at the FB pin is 1.26V. Pick R_{F1} (the resistor between the output voltage and the feedback pin) and R_{F2} (the resistor between the feedback pin and ground) can be selected using the following equation,

$$R_{F2} = (1.26V \times R_{F1}) / (V_{out} - 1.26V) \quad (15)$$

A 100pF capacitor may be connected between the feedback and ground pins to reduce noise.

SETTING THE CURRENT LIMIT

The maximum amount of current that can be delivered to the load is set by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. When this threshold is reached, the switch will be turned off until the next cycle. Limits for V_{SENSE} are specified in the electrical characteristics section. V_{SENSE} represents the maximum value of the internal control signal V_{CS} as shown in Figure 33. This control signal, however, is not a constant value and changes over the course of a period as a result of the internal compensation ramp (V_{SL}). Therefore the current limit threshold will also change. The actual current limit threshold is a function of the sense voltage (V_{SENSE}) and the internal compensation ramp:

$$R_{SEN} \times ISW_{LIMIT} = VCS_{MAX} = V_{SENSE} - (D \times V_{SL}) \quad (16)$$

Where ISW_{LIMIT} is the peak switch current limit, defined by the equation below.

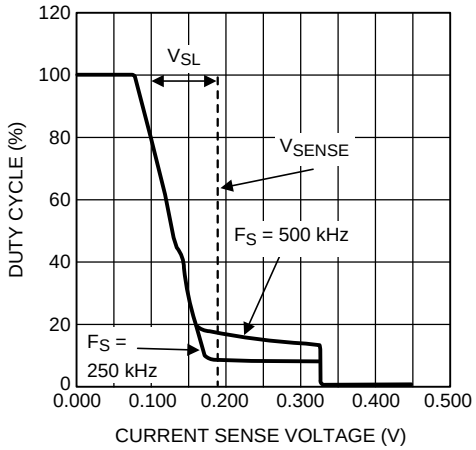


Figure 33. Current Sense Voltage vs Duty Cycle

Figure 33 shows how V_{CS} (and current limit threshold voltage) change with duty cycle. The curve is equivalent to the internal compensation ramp slope (S_e) and is bounded at low duty cycle by V_{SENSE}, shown as a dotted line. As duty cycle increases, the control voltage is reduced as V_{SL} ramps up. The graph also shows the short circuit current limit threshold of 343 mV (typical) during the 325 ns (typical) blanking time. For higher frequencies this fixed blanking time obviously occupies more duty cycle, percentage wise. Since current limit threshold varies with duty cycle, the following equation should be used to select R_{SEN} and set the desired current limit threshold:

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SL})}{ISW_{LIMIT}} \quad (17)$$

The numerator of the above equation is V_{CS}, and ISW_{LIMIT} is calculated as:

$$ISW_{LIMIT} = \left[\frac{I_{OUT}}{(1-D)} + \frac{(D \times V_{IN})}{(2 \times f_S \times L)}\right] \quad (18)$$

To avoid false triggering, the current limit value should have some margin above the maximum operating value, typically 120%. Values for both V_{SENSE} and V_{SL} are specified in Electrical Characteristics. However, calculating with the limits of these two specs could result in an unrealistically wide current limit or R_{SEN} range. Therefore, the following equation is recommended, using the V_{SL} ratio value given in Electrical Characteristics:

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SENSE} \times V_{SL}ratio)}{ISW_{LIMIT}} \quad (19)$$

R_{SEN} is part of the current mode control loop and has some influence on control loop stability. Therefore, once the current limit threshold is set, loop stability must be verified. As described in the slope compensation section, the following must hold true for a current mode converter to be stable:

$$S_f - S_e < S_n + S_e \quad (20)$$

To verify that this equation holds true, use the following equation:

$$R_{SEN} < \frac{2 \times V_{SL} \times f_S \times L}{Vo - (2 \times V_{IN})} \quad (21)$$

If the selected RSEN is greater than this value, additional slope compensation must be added to ensure stability, as described in the section below.

CURRENT LIMIT WITH EXTERNAL SLOPE COMPENSATION

R_{SL} is used to add additional slope compensation when required. It is not necessary in most designs and R_{SL} should be no larger than necessary. Select RSL according to the following equation:

$$R_{SL} > \frac{\frac{R_{SEN} \times (Vo - 2V_{IN})}{2 \times f_S \times L} - V_{SL}}{40\ \mu A} \quad (22)$$

Where R_{SEN} is the selected value based on current limit. With RSL installed, the control signal includes additional external slope to stabilize the loop, which will also have an effect on the current limit threshold. Therefore, the current limit threshold must be re-verified, as illustrated in the equations below :

$$V_{CS} = V_{SENSE} – (D \times (V_{SL} + \Delta V_{SL})) \quad (23)$$

Where ΔV_{SL} is the additional slope compensation generated as discussed in the slope compensation ramp section and calculated as:

$$\Delta V_{SL} = 40\ \mu A \times R_{SL} \quad (24)$$

This changes the equation for current limit (or R_{SEN}) to:

$$ISW_{LIMIT} = \frac{V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL}))}{R_{SEN}} \quad (25)$$

The R_{SEN} and R_{SL} values may have to be calculated iteratively in order to achieve both the desired current limit and stable operation. In some designs R_{SL} can also help to filter noise on the I_{SEN} pin.

If the inductor is selected such that ripple current is the recommended 30% value, and the current limit threshold is 120% of the maximum peak, a simpler method can be used to determine R_{SEN}. The equation below will provide optimum stability without RSL, provided that the above 2 conditions are met:

$$R_{SEN} = \frac{V_{SENSE}}{ISW_{LIMIT} + \left(\frac{Vo - Vi}{L \times f_S}\right) \times D} \quad (26)$$

POWER DIODE SELECTION

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using the formula:

$$I_{D(Peak)} = I_{OUT} / (1−D) + \Delta I_L \quad (27)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

POWER MOSFET SELECTION

The drive pin of the LM3478 must be connected to the gate of an external MOSFET. The drive pin (DR) voltage depends on the input voltage (see typical performance characteristics). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub logic level MOSFET should be used. The selected MOSFET has a great influence on the system efficiency. The critical parameters for selecting a MOSFET are:

1. Minimum threshold voltage, V_{TH}(MIN)
2. On-resistance, $R_{DS(ON)}$
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}
5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. Vds(max) must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and switching losses. Rds(on) is needed to estimate the conduction losses, Pcond:

$$Pcond = I^2 \times R_{DS(ON)} \times D \tag{28}$$

The temperature effect on the $R_{DS(ON)}$ usually is quite significant. Assume 30% increase at hot.

For the current I in the formula above the average inductor current may be used.

Especially at high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often the individual MOSFET's data sheet does not give enough information to yield a useful result. The following formulas give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{Lmax} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL}) \tag{29}$$

$$t_{LH} = \left(Qgd + \frac{Qgs}{2}\right) \times \frac{Rdr_{On}}{Vdr - Vgs_{th}} \tag{30}$$

INPUT CAPACITOR SELECTION

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular as shown in Figure 32. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \frac{1}{2\sqrt{3}} \left(\frac{V_{OUT} - V_{IN}}{V_{OUT} L f_S}\right) \times V_{in} \tag{31}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10µF to 20µF. If a value lower than 10µF is used, then problems with impedance interactions or switching noise can affect the LM3478. To improve performance, especially with Vin below 8 volts, it is recommended to use a 20 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly (see Figure 34). A 0.1µF or 1µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

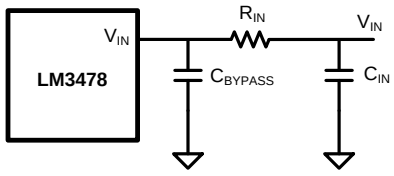


Figure 34. Reducing IC Input Noise

OUTPUT CAPACITOR SELECTION

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum RMS current. The RMS current in the output capacitor is:

$$I_{COUT(RMS)} = \sqrt{(1-D)\left[I_{OUT}^2 \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]} \quad (32)$$

Where

$$\Delta i_L = \frac{DV_{IN}}{2Lf_S} \quad (33)$$

The ESR and ESL of the capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic, polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

For applications that require very low output voltage ripple, a second stage LC filter often is a good solution. Most of the time it is lower cost to use a small second Inductor in the power path and an additional final output capacitor than to reduce the output voltage ripple by purely increasing the output capacitor without an additional LC filter.

LAYOUT GUIDELINES

Good board layout is critical for switching controllers. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switching converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted Ldi/dt noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily affected by switching noise. This noise can cause duty cycle jittering which leads to increased spectral noise. Although the LM3478 has 325ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time.

The most important layout rule is to keep the AC current loops as small as possible. Figure 35 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted lined traces of the bottom schematic are the once to make as short as possible.

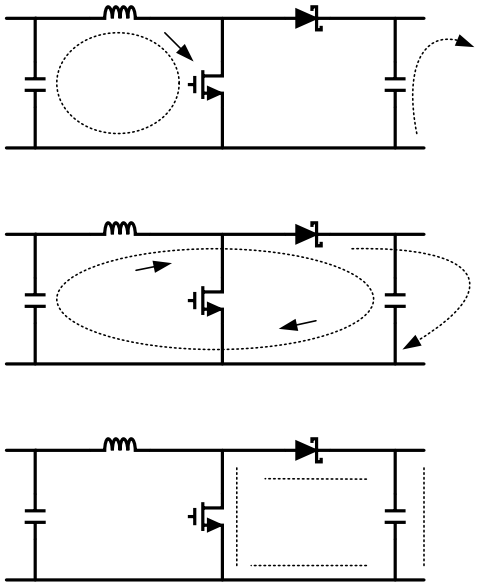


Figure 35. Current Flow In A Boost Application

The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents, attach all the grounds of the system only at one point.

A ceramic input capacitor should be connected as close as possible to the Vin pin and grounded close to the GND pin.

For a layout example please see AN-1204. For more information about layout in switch mode power supplies please refer to AN-1229.

COMPENSATION

For detailed explanation on how to select the right compensation components to attach to the compensation pin for a boost topology please see AN-1286.

Designing SEPIC Using the LM3478

Since the LM3478 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of a SEPIC using the LM3478 is shown in Figure 36. Note that the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled inductor since equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom inductor. The input ripple can be reduced along with size by using the coupled windings for L1 and L2.

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of a SEPIC over a boost converter is the inherent input to output isolation. The capacitor CS isolates the input from the output and provides protection against a shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given by:

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \quad (34)$$

In the above equation, V_Q is the on-state voltage of the MOSFET, Q, and V_{DIODE} is the forward voltage drop of the diode.

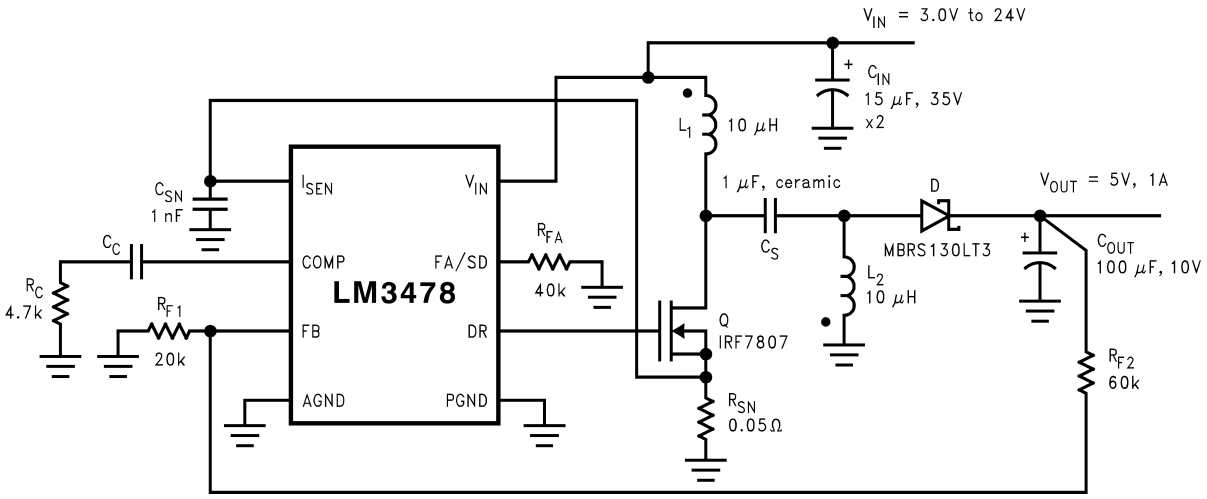


Figure 36. Typical SEPIC Converter

POWER MOSFET SELECTION

As in a boost converter, parameters governing the selection of the MOSFET are the minimum threshold voltage, $V_{TH(MIN)}$, the on-resistance, $R_{DS(ON)}$, the total gate charge, Q_g, the reverse transfer capacitance, C_{RSS}, and the maximum drain to source voltage, $V_{DS(MAX)}$. The peak switch voltage in a SEPIC is given by:

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE} \quad (35)$$

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)} \quad (36)$$

The peak switch current is given by:

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2} \quad (37)$$

The RMS current through the switch is given by:

$$I_{SWRMS} = \sqrt{\left[I_{SWPEAK}^2 - I_{SWPEAK}\left(\Delta I_{L1} + \Delta I_{L2}\right) + \frac{\left(\Delta I_{L1} + \Delta I_{L2}\right)^2}{3}\right] D} \quad (38)$$

POWER DIODE SELECTION

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is $V_{IN} + V_{OUT}$. Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

SELECTION OF INDUCTORS L1 AND L2

Proper selection of inductors L1 and L2 to maintain continuous current conduction mode requires calculations of the following parameters.

Average current in the inductors:

$$I_{L1AVE} = \frac{DI_{OUT}}{1\text{-}D} \quad (39)$$

$$I_{L2AVE} = I_{OUT} \quad (40)$$

Peak to peak ripple current, to calculate core loss if necessary:

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{(L1) f_S} \quad (41)$$

$$\Delta I_{L2} = \frac{(V_{IN} - V_Q)\, D}{(L2) f_S} \quad (42)$$

Maintaining the condition $I_L > \Delta i_L/2$ to ensure continuous current conduction yields:

$$L1 > \frac{(V_{IN} - V_Q)(1-D)}{2 I_{OUT} f_S} \quad (43)$$

$$L2 > \frac{(V_{IN} - V_Q) D}{2 I_{OUT} f_S} \quad (44)$$

Peak current in the inductor, to ensure the inductor does not saturate:

$$I_{L1PK} = \frac{D I_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2} \quad (45)$$

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2} \quad (46)$$

I_{L1PK} must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended to reduce input ripple and output ripple. However, once D_{IL1} is less than 20% of I_{L1AVE}, the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommended, Δ_{IL2} can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left(\frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) \text{ESR} \quad (47)$$

where ESR is the effective series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then L1 = L2 = L. All the equations above will hold true if the inductance is replaced by 2L.

SENSE RESISTOR SELECTION

The peak current through the switch, $I_{SW(PEAK)}$ can be adjusted using the current sense resistor, R_{SEN}, to provide a certain output current. Resistor R_{SEN} can be selected using the formula:

$$R_{SEN} = \frac{V_{SENSE} - D(V_{SL} + \Delta V_{SL})}{I_{SWPEAK}} \quad (48)$$

Sepic Capacitor Selection

The selection of the SEPIC capacitor, CS, depends on the RMS current. The RMS current of the SEPIC capacitor is given by:

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + \left(I_{L1PK}^2 - I_{L1PK} \Delta I_{L1} + \Delta I_{L1}^2 \right)(1-D)} \quad (49)$$

The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. There is an energy balance between CS and L1, which can be used to determine the value of the capacitor. The basic energy balance equation is:

$$\frac{1}{2} C_S \Delta V_S^2 = \frac{1}{2} L_1 \Delta I_{L1}^2 \quad (50)$$

where

$$\Delta V_S = \left(\frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}}\right) \frac{I_{OUT}}{f_S C_S} \quad (51)$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q)\, D}{L_1 f_S} \quad (52)$$

is the ripple current through the inductor L1. The energy balance equation can be solved to provide a minimum value for C_S:

$$C_S \geq L_1 \frac{{I_{OUT}}^2}{(V_{IN} - V_Q)^2} \quad (53)$$

Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given by:

$$I_{CIN(RMS)} = \Delta I_{L1} / \sqrt{12} = \frac{D}{2\sqrt{3}} \left(\frac{V_{IN} - V_Q}{L_1 f_S}\right) \quad (54)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10µF to 20µF. If a value lower than 10µF is used than problems with impedance interactions or switching noise can affect the LM3478. To improve performance, especially with V_{IN} below 8 volts, it is recommended to use a 20Ω resistor at the input to provide a RC filter. The resistor is placed in series with the V_{IN} pin with only a bypass capacitor attached to the V_{IN} pin directly (see Figure 34). A 0.1µF or 1µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

Output Capacitor Selection

The output capacitor of the SEPIC sees very large ripple currents (similar to the output capacitor of a boost converter). The RMS current through the output capacitor is given by:

$$I_{RMS} = \sqrt{\left[{I_{SWPK}}^2 - I_{SWPK} (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3}\right] (1\text{-}D) - {I_{OUT}}^2} \quad (55)$$

The ESR and ESL of the output capacitor directly control the output ripple. Use low capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo-OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

Other Application Circuits

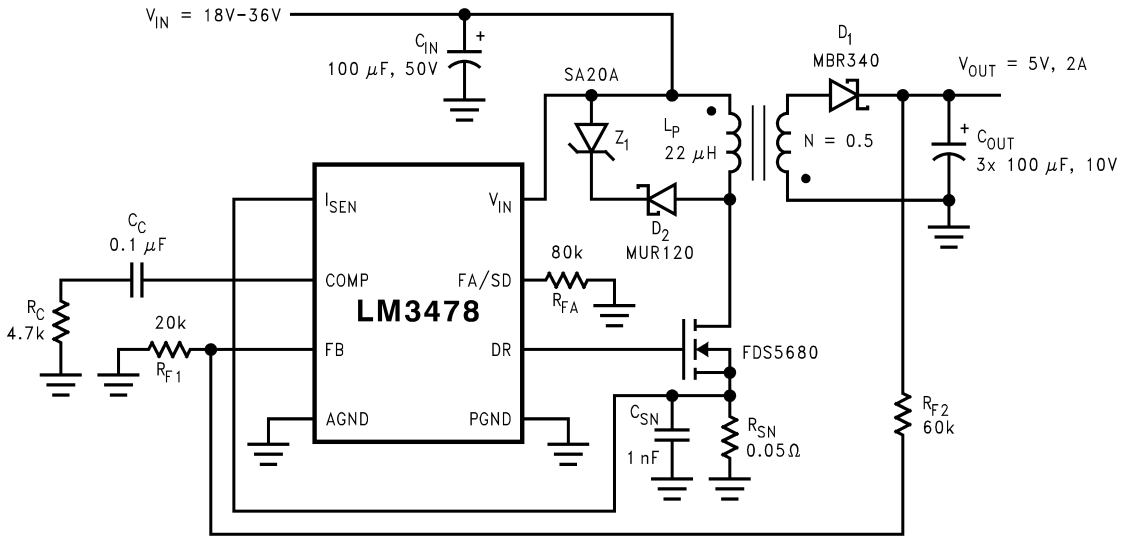


Figure 37. Typical Flyback Circuit

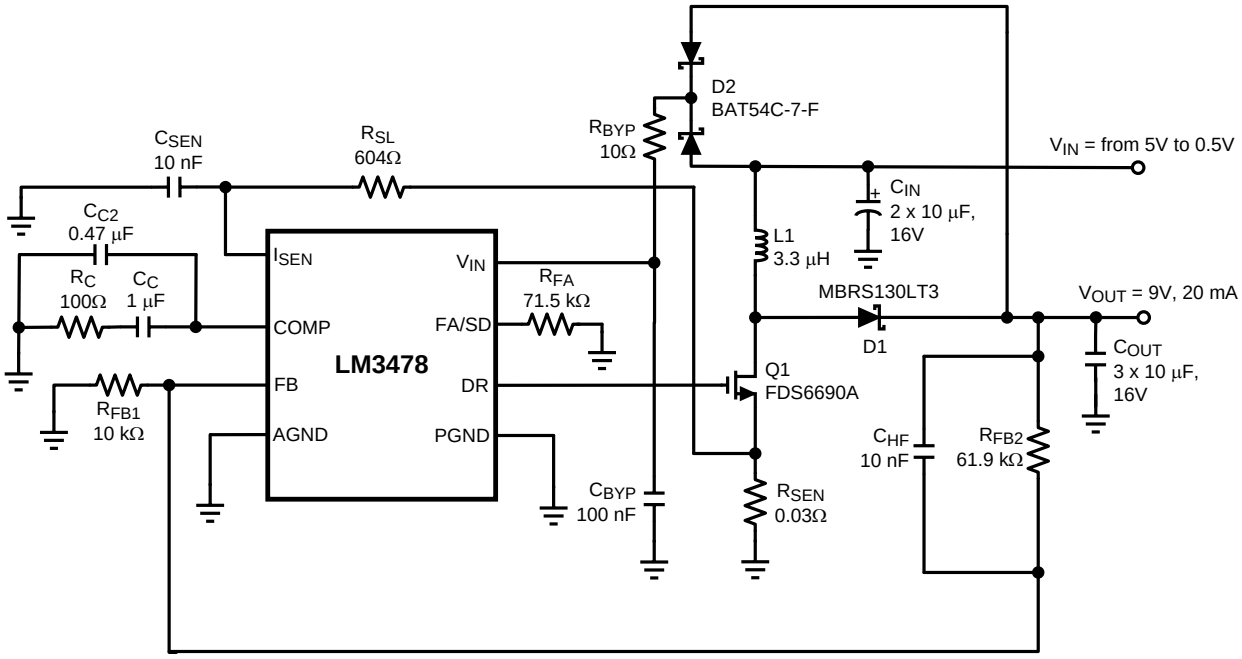


Figure 38. Back Powering Circuit for Vin < 3V (>3V input needed for startup)

REVISION HISTORY

Changes from Revision U (February 2013) to Revision V	Page
• Changed layout of National Data Sheet to TI format	24

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3478MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3478 MA	Samples
LM3478MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		L3478 MA	Samples
LM3478MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	S14B	
LM3478MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S14B	Samples
LM3478MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S14B	Samples
LM3478QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SSFB	Samples
LM3478QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	SSFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

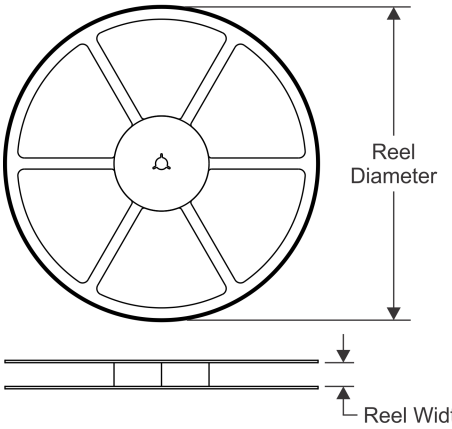
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

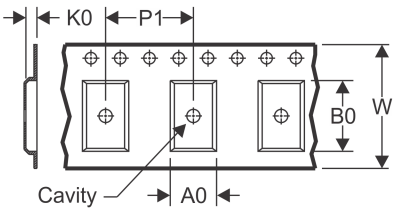
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

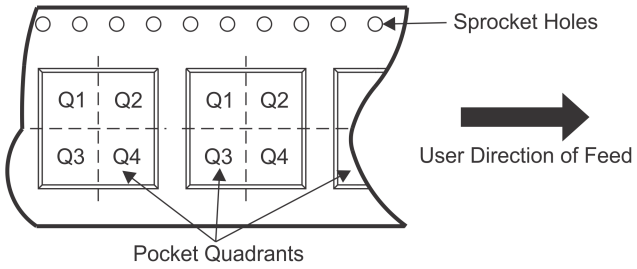


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

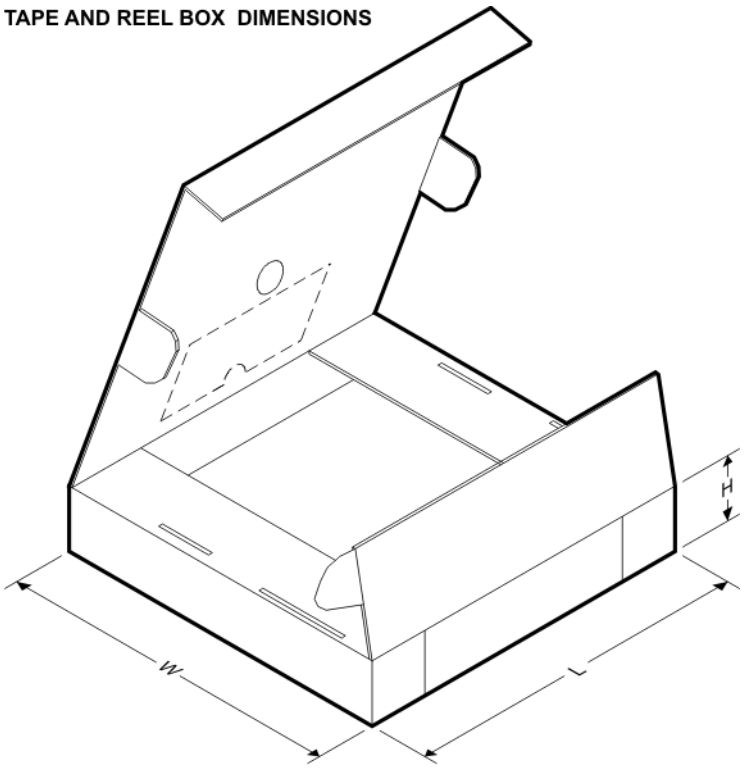
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3478MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM3478MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3478MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3478MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3478QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3478QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

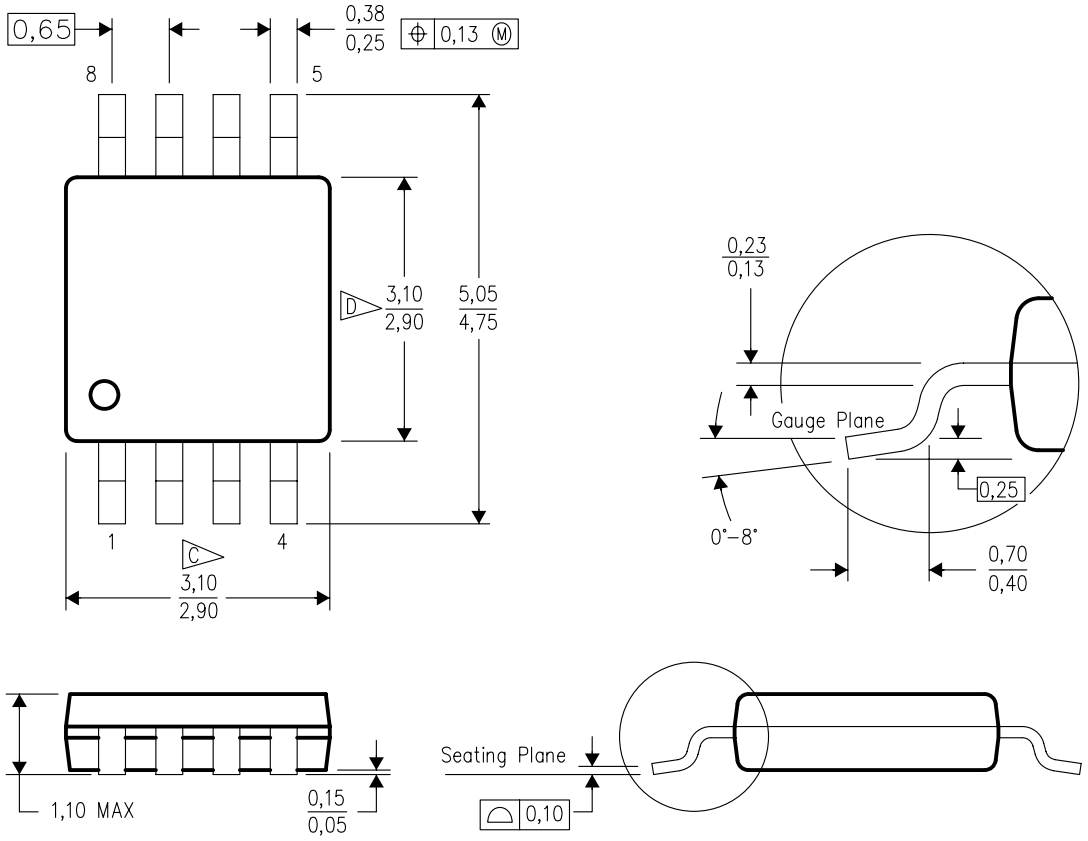
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3478MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM3478MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3478MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3478MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3478QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3478QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

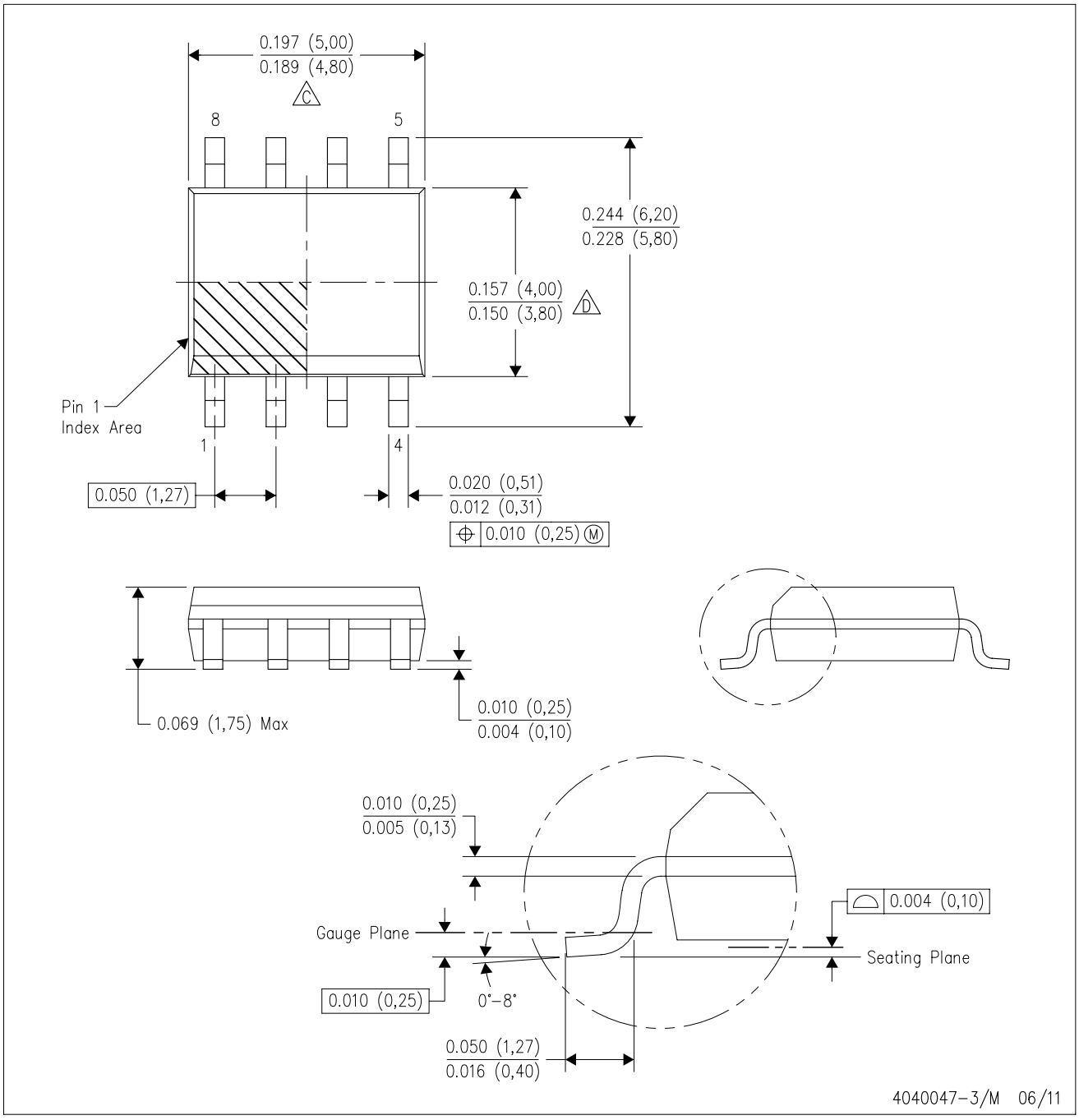
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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